analog dialogue

A forum for the exchange of circuits and systems for real-world signal processing

QUAD 8-BIT CMOS DAC WITH BUFFERED VOLTAGE OUTPUTS **(see page 3)**

Avoiding Passive-Component Pitfalls (page 6)

Designing Digital FIR Filters (page 12)

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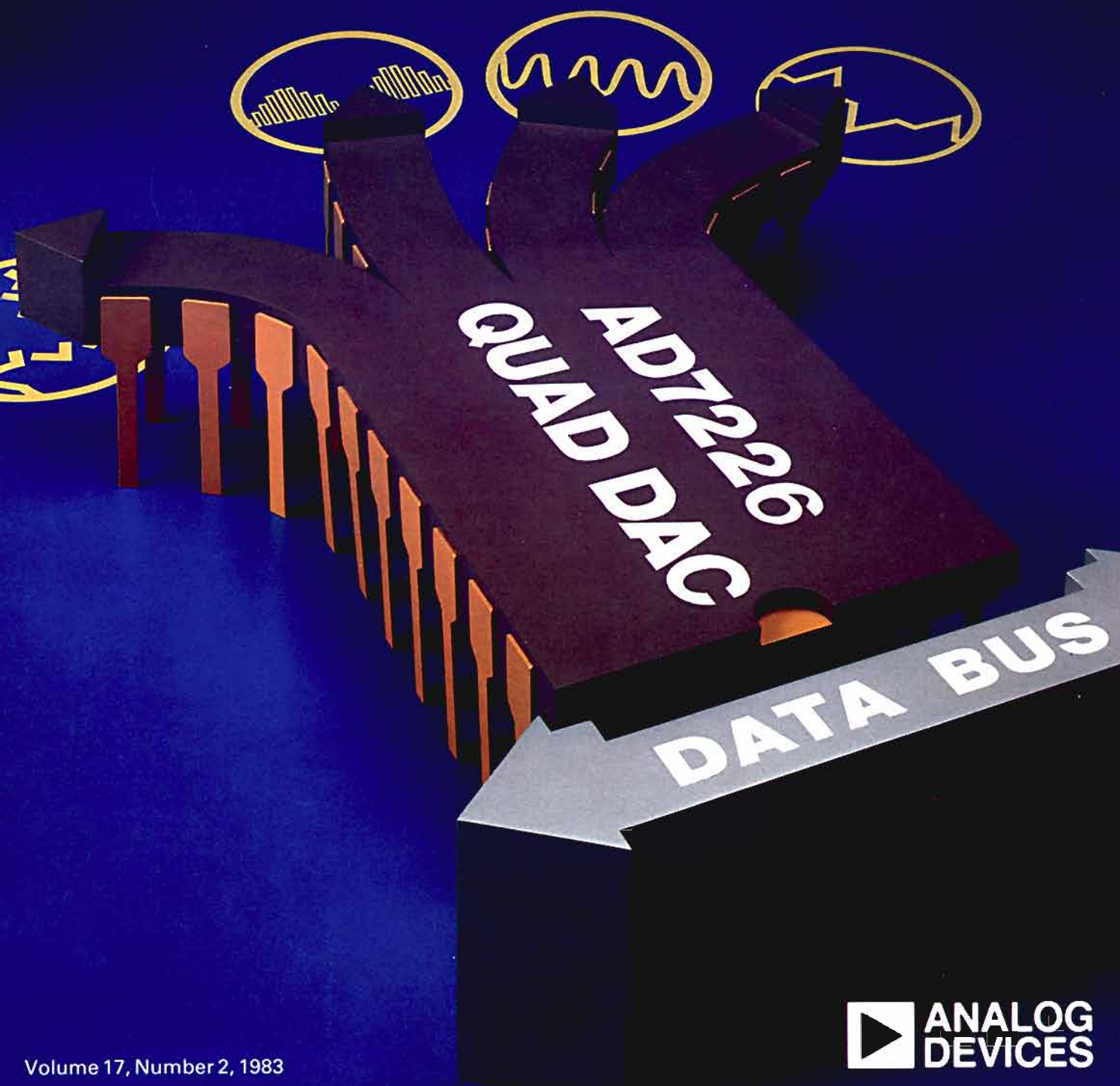

Volume 17, Number 2, 1983

ANALOG DEVICES

Editor's Notes

DISCOURAGED?

Readers may notice that we've followed up the articles (in the last two issues) on the anticipation and cure of interference noise with an article in the current issue on the quirks of passive components. Like the substance of the seminars given by our applications engineers, it's certainly useful stuff.

But the report of one of our application engineers after some recent seminar tours gives us some qualms. After several hours of giving the inside story on analog circuit design, punctuated by examples of classic discrepancies between functional block diagrams and real circuits, he was approached by one or two members of the audience, who said (in effect), "This is just too frightening. I think I'll go back to software design."

Are our efforts self-defeating? Are we giving our readers such a heavy dosage of the seamy side of life in systems and on the circuit board that we are actually killing interest in analog circuit design among some of the very people we want to attract to it?

Are we being a little like the metropolitan newspapers which, by incessant and lurid reports on crime in the city, drive away potential visitors and future residents? For the vast majority of visitors and residents, those who take a few simple precautions can have a wonderful time in most parts of the city; a few others, who must go to crime-ridden areas to seek their reward, have to be much more careful, but they will be rewarded for their care.

Similarly, the requirements of a large number of applications don't call for much more than common sense and remembering a few basic rules (repeated in various guises throughout the series of articles). Most good engineers can design circuits to meet those requirements with little effort—and an occasional backward glance. It's usually only when high precisions are needed, and/or the environment becomes crowded with circuits and with large and small signals at a variety of frequencies, that the utmost of care, plus experience, clear thinking, and exposure to useful hints, such as those published here—as well as some trial-and-error—are needed to insure survival.

Furthermore, remember that these articles are a form of cumulative wisdom representing individual experiences plucked from untold manhours of expert design time, in learning how to avoid muggings in various places from the cathedrals to the "Hell's Kitchens" of Design City. Remember too that no designer ever gets to be so smart and cautious that (s)he doesn't suffer an occasional mugging in some creative new way. We invite you to write us, for the benefit of other readers, some of the things *you've* found out the hard way about the successful design of analog circuits.

This diversity of design problems, coupled with the diversity of design talents among our readers, is one of the factors that has impelled Analog Devices to seek to offer a fully integrated gamut of products to deal with real-world signals, from ICs for economy-minded design experts to MACSYM measurement-and-control systems for people who would avoid system design headaches—and from analog signal conditioners to digital signal processors. ▶

Dan Sheingold

THE AUTHORS

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Doug Grant (page 6), New-Product Marketing Manager for data converters at Analog Devices Semiconductor, gained substantial recognition as a Microcircuits Application Engineer at ADS and has won "best paper" awards at several IEEE conferences. He has a BSEE from Lowell Technological Institute and extensive experience in developing converters, μP-based data-acquisition systems, and analytical instruments. He is also active in Amateur Radio.

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FOUR BUFFERED VOLTAGE-OUT 8-BIT DACS IN ONE 20-PIN DIP

Industry's First Monolithic Quad DAC Saves Time, Space, & Money

AD7226 Has Fast Response, Tracking Characteristics, 0.3" Footprint

by Paschal Minogue, Mike Byrne, and John Jennings

In 1973, Analog Devices introduced the world's first CMOS multiplying DAC, the instantly (and still) popular AD7520.* It is a switched ten-tap R-2R network, with neither analog nor digital buffering. Now, a decade later, and still first, Analog Devices has introduced the AD7226,* which comprises four 8-bit DACs on a single CMOS silicon chip in a 20-pin dual in-line package; they share a common digital bus via addressable latches and have four buffered analog voltage outputs (Figure 1).

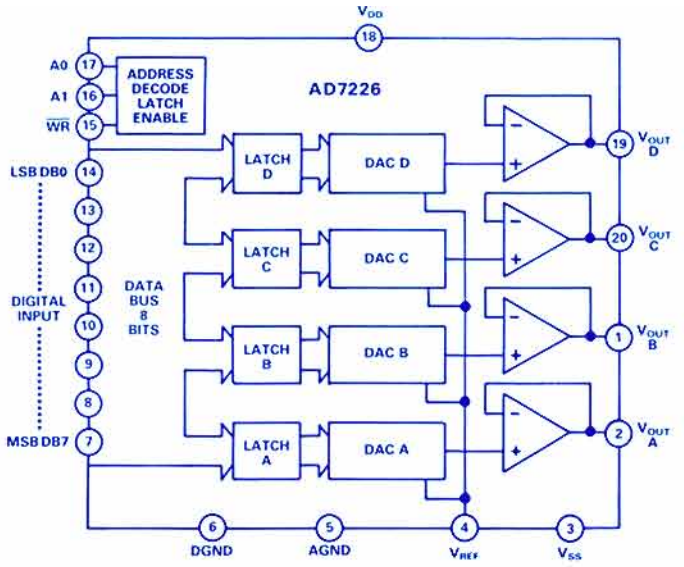


Figure 1. Functional block diagram of the AD7226.

WHY QUADS?

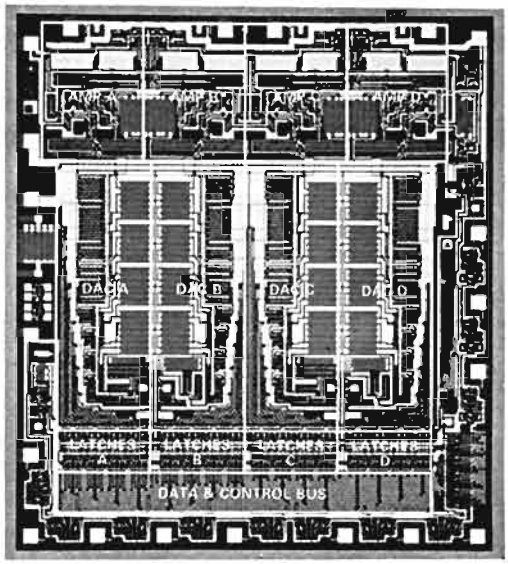
Because each decoder line doubles the number of channels the bus can communicate with, multiple DACs start out as duals (like the AD7528*); and the quad is the next sensible step.

Where would sets of four 8-bit DACs be used? First and foremost, they would be used for their economy in systems and equipment employing large numbers of DACs (if a quad with *12-bit* resolution is needed, the hybrid AD390* is available). The advantages begin with low per-channel cost for the device itself; in addition, the AD7226 occupies only one 0.3" 20-pin DIP location—replacing 4 single DACs, a quad buffer op amp, four latches, and an external 4-channel decoder. This combination of advantages saves design time, parts cost, and precious "real estate", and it provides logistical savings at all stages of production of the user's equipment or system.

Since all four of the DACs are fabricated at the same time and on the same chip, their linearity, gain accuracy, etc., have an inherent tendency to be matched and to track well with temperature.

DACs purchased in sets of four can be used in applications calling for outputs in pairs, triads, and quads, for example, to set references in 2-, 4-, 6-, or 8-level window comparators. Displays and multi-axis controls also come to mind. The on-board DACs can

*For technical data, use the reply card.



also be used in pairs, with a high-accuracy reference DAC and an ADC, to furnish arbitrary numbers of voltages with accuracies and resolutions of up to 12 or more bits at low cost in servoed operation.

ANATOMY OF A QUAD DAC

The four sets of latches are loaded via a common 8-bit data bus, under the control of two address bits (A0, A1) and an active low WRITE pin ($\overline{WR}$). All logic inputs are level-triggered and compati-

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ble with both TTL and CMOS (5-V). Because its logic-interface circuitry operates at high speed, the AD7226 is compatible with most 8-bit microprocessors; typically, all four channels can be updated at 2 MHz, and a single channel can be updated at 8 MHz.

The converter consists of an 8-bit R-2R ladder and its associated switches, connected for operation in the voltage mode (Figure 2). The output of each DAC is buffered by a short-circuit protected on-chip CMOS follower amplifier, capable of driving up to 5 mA of output current. Because the device operates in the voltage mode, with non-inverting buffers, a single supply (V_{DD}) from +11.4 V to +16.5 V may be used for unipolar output. The table shows the reference and output ranges for linear operation at each nominal supply-voltage level. Bipolar operation of the individual DACs is easily achieved with the addition of one external amplifier and 2 matched resistors.

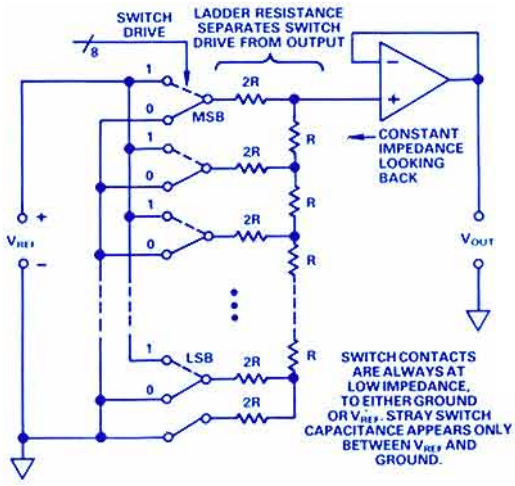


Figure 2. Functional diagram of one DAC Section.

V_{DD}	V_{REF} LIMIT LOWER	V_{REF} LIMIT UPPER	OUTPUT RANGE
15V ± 10%	+2 V	+10 V	0 TO +10 V
12V ± 5%	+2 V	+7.5 V	0 TO +7.5 V

Most of today's CMOS digital-to-analog converters are wired so that they may be used in either the current-switching mode (Figure 3) or the voltage-switching mode, depending on how the reference, the output terminal, the LSB termination, and the op amp are connected. In order to provide our users with a unit having the minimum number of pins, we chose the dedicated voltage mode, sacrificing some flexibility. However, in addition to single-supply capability and a smaller footprint, this choice led to significant further advantages in speed and linearity.

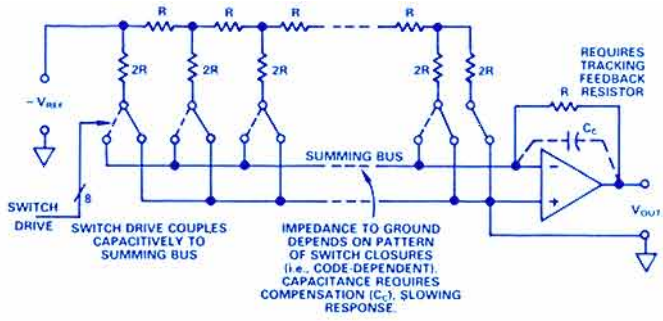
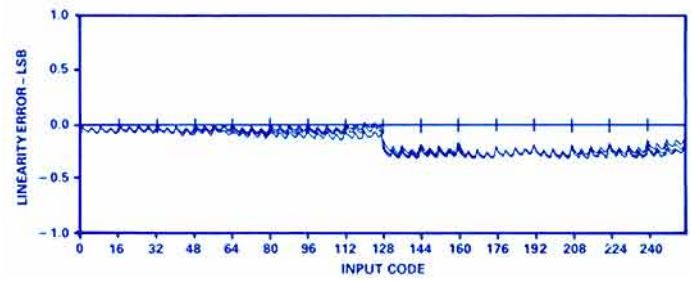


Figure 3. A typical CMOS DAC connected for current output, showing sources of dynamic and linearity error.

Speed is improved over that of current-mode DACs because the switch capacitance, which is both high (tens of picofarads) and variable, loads the low-impedance reference circuit, rather than the high-impedance summing point. Similarly, the output waveform of the DAC is cleaner, because feedthrough via switch capacitance is sunk in the low-impedance external reference and not coupled to the output. Settling time of output voltage to ± ½ LSB is about 4 μs for a 10-V step change.

Differential linearity is improved, because the code-dependent variable resistance seen by the low-impedance reference source does not cause the offset to be modulated by the code-dependent noise gain of the buffer-amplifier circuit as it does in the current-output configuration; hence any amplifier offsets remain constant offsets instead of becoming sources of nonlinearity as well. Figure 4 shows a plot of linearity error for a typical AD7226 DAC. The errors for all four DACs are superimposed to demonstrate the close degree of tracking.



(a) Superimposed linearity errors of all four DACS.

	DAC A	DAC B	DAC C	DAC D
ZERO CODE (OFFSET) – mV	1.85	2.65	2.58	2.95
MAX/MIN ERROR – LSB	0.04 – 0.32	0.01 – 0.31	0.01 – 0.32	0 – 0.31
MAX DIFF. ERROR – LSB	–0.21	–0.16	–0.14	0.11
FULL-SCALE (GAIN) ERROR – LSB	–0.17	–0.21	–0.21	–0.23

(b) Offset and range errors at +25°C, V_{DD} = 14.952V, V_{SS} = −5.0339V, V_{REF} = 9.9869V, 1 LSB = 39mV.

Figure 4. Errors of an AD7226 Quad DAC.

The AD7226 is fabricated in a new all ion-implanted high-speed linear-compatible CMOS ("LC^2 MOS") process, which has been developed specifically to permit high-speed digital logic circuits and precise analog circuits to be integrated onto the same chip. The photograph on page 3 shows how the small 140 x 125-mil chip is partitioned. The analog output circuitry is at one end of the die, and the data and control buses are at the other end.

Benefits of the LC^2 MOS process in the AD7226 include fast dense logic and CMOS amplifiers with good performance. The process has also been used for the AD7240, a fast pretrimmed 12-bit DAC* (*Analog Dialogue* 16-3, 1982, page 22) with low propagation delay and low digital charge injection, and for a number of products now in planning, development, and pilot production.

APPLICATIONS

The AD7226 is useful wherever multiple voltages must be independently set by a digital source with resolutions of up to 1 part in 256. Examples include direct or incremental setting of test voltages, digital system-trim adjustments, setting of window widths in comparator applications, digital generation of multi-phase (e.g., 3-phase) sine waves, and setting of constants in analog computing circuits. Other applications might include adjustment of variable-capacitor voltage to tune multistage radio-frequency stages of VHF and UHF receivers optimally under microprocessor control.

Bipolar Operation. The unipolar voltage range of any of the AD7226's d/a converters can be rendered bipolar by connecting an external op amp for a gain of 2 and subtracting the reference voltage, as shown in Figure 5. If necessary, the reference voltage and the gain can be adjusted to trim the offset and scale factor.

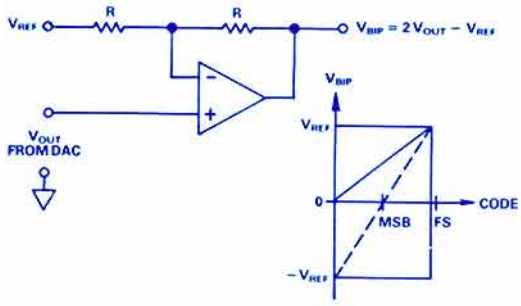


Figure 5. An external op amp converts a DAC from single-ended to bipolar.

Digitally Controlled Common Reference. One of the DACs in an AD7226 may be used in a feedback configuration to control the reference voltage for itself and the other DACs in one or more AD7226's. A difference configuration, like that shown in Figure 6, provides a positive reference.

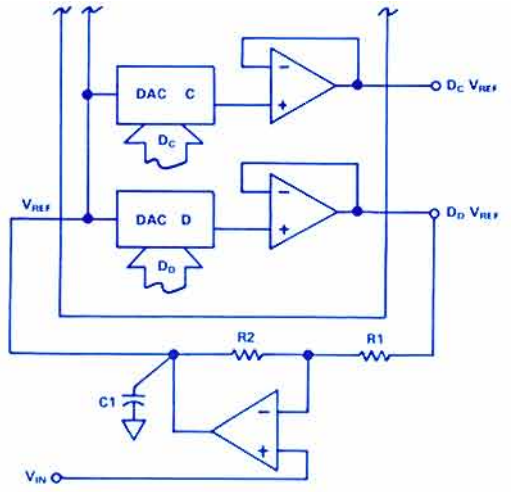


Figure 6. Digitally adjustable common reference.

In Figure 6, the output of the DAC is equal to D V_{REF}, where D is the fractional (integer/2^n) binary equivalent of the 8-bit input word and V_{REF} is the voltage at the output of the op amp. The op amp is amplifying the reference input voltage, V_{IN}, by $(1 + R_2/R_1)$, and adding to it $(-R_2/R_1)\,D\,V_{REF}$. Thus,

$$V_{REF} = V_{IN}\left(1 + \frac{R_2}{R_1}\right) - D\,V_{REF}\left(\frac{R_2}{R_1}\right) \qquad (1)$$

hence,

$$V_{REF} = V_{IN}\,\frac{\left(1 + \frac{R_2}{R_1}\right)}{\left(1 + D\,\frac{R_2}{R_1}\right)} \qquad (2)$$

The range of adjustment is from $V_{REF} = V_{IN}\,(1 + R_2/R_1)$, for D = 0, to $V_{REF} \approx V_{IN}$, for D = 255/256.

For a given V_{IN} and resistance ratio, since the gain is digitally adjusted, the computer can use (3) to calculate the required value of D for a given value of V_{REF}:

$$D = \frac{V_{IN}}{V_{REF}}\left(1 + \frac{R_1}{R_2}\right) - \frac{R_1}{R_2} \qquad (3)$$

Since the reference lines of all four DACs are connected to the same input terminal, they will all have the same full-scale output. If more than one AD7226 is used, the reference lines of all devices can be connected together to obtain a common controllable tracking reference. The circuit's gain, with $R_{FB} = 3R$, allows 10-volt full-scale reference voltage to be obtained with a 2.5-volt reference (e.g., the AD580* or AD1403*). Stability, response speed, and noise reduction of the circuit are controlled by the choice of capacitor C1.

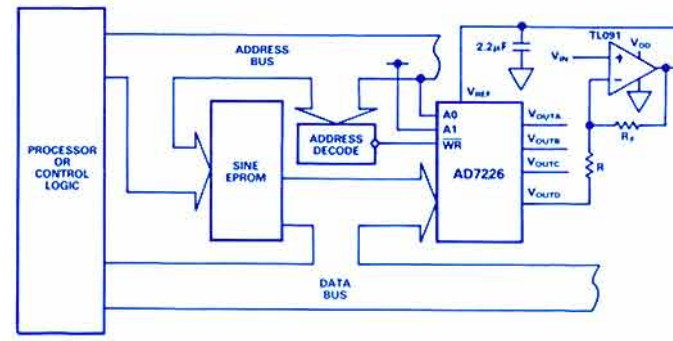


Figure 7. 3-Phase Sine Wave Generator Circuit.

Three-phase sine generator. Figure 7 shows an application of the AD7226 in the generation of 3-phase sine waves. The required phase shift of 120° between the three d/a-converter outputs is generated in software. The sine EPROM contains a full sine-wave lookup table. Data is loaded into the three DACs from the sine EPROM.

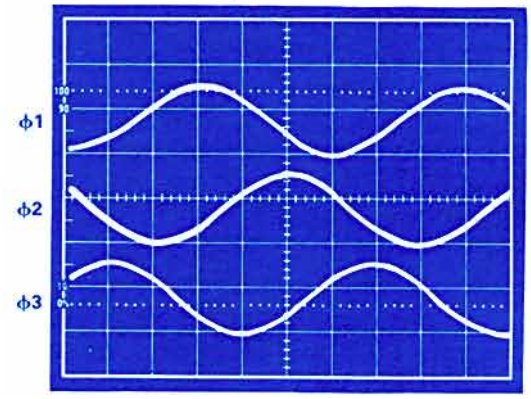


Figure 8. Waveforms in 3-phase sine generator.

Three loops are generated in software, producing successive triads of angle values with 120° separation at each increment of angular rotation. These values, which correspond to angular inputs to the lookup table, produce sinusoidal outputs which are used to load the DACs. Each DAC is fed from a separate loop, resulting in 3 sine-wave voltages, 120° out of phase, at each increment of angular rotation. The sine waves can be smoothed by interposing simple filters between the DAC outputs and the signal destinations. Figure 8 shows typical resulting waveforms.

The 4-channel AD7226, a low-cost compact 8-bit voltage-output device with good tracking, should find many applications in the design of instruments, systems, and equipment.

AVOIDING PASSIVE-COMPONENT PITFALLS

The Wrong Passive Component Can Derail Even the Best Op Amp or Data Converter Here Are Some Basic Traps to Watch for.

by Doug Grant and Scott Wurcer

You've just spent $25 or more for a precision op amp or data converter, only to find that, when plugged into your board, the device doesn't meet spec. Perhaps the circuit suffers from drift, poor frequency response, oscillations—or simply doesn't achieve the accuracy you expect. Well, before you blame the device itself, you should examine your passive components—including capacitors, resistors, potentiometers, and yes, even the printed circuit boards themselves. Subtle effects of tolerance, temperature, parasitics, aging, and user assembly procedures can unwittingly sink your circuit. And these effects all too often go unspecified or underspecified by manufacturers.

In general, if you use data converters having 12 bits or more of resolution, or op amps that cost more than $5, you should pay particularly close attention to passive-component selection. To put the problem in perspective, consider the case of a 12-bit digital-to-analog converter (DAC). One half LSB (least-significant bit) corresponds to 0.012% of full scale, or only 122 parts per million (ppm)! The host of passive-component phenomena can quickly accumulate errors far exceeding this level.

Buying the most-expensive passive components won't necessarily solve your problems either. Often, the correct 25-cent capacitor will yield a better-performing, more cost-effective design than the premium-grade $8 part. Although not necessarily easy, understanding and analyzing passive-component effects may prove quite rewarding, once you understand a few basics.

CAPACITORS

Most designers are generally familiar with the range of capacitors available. But the mechanisms by which both static and dynamic errors can occur in precision circuit designs are easy to forget because of the tremendous variety of capacitor types, e.g.: glass, aluminum foil, solid tantalum and tantalum foil, silver mica, ceramic, Teflon, and the film capacitors, including polyester, polycarbonate, polystyrene, and polypropylene types.

Figure 1 is a workable model of a non-ideal capacitor. The nominal capacitance, C, is shunted by a resistance R_p, representing insulation resistance or leakage. A second resistance, R_s—equivalent series resistance, or ESR—appears in series with the capacitor and represents the resistance of the leads and capacitor plates.* Inductance, L—the equivalent series inductance, or ESL, models the inductance of the leads and plates. Finally, resistance R_{da} and capacitance C_{da} together form a simplified model of a phenomenon

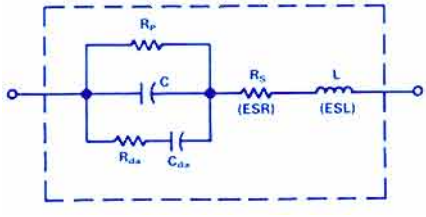


Figure 1. Capacitor equivalent circuit.

*Capacitor phenomena aren't that easy to separate out. This matching of phenomena and models is for convenience in explanation.

non known as dielectric absorption. Dielectric absorption can ruin the dynamic performance of both fast and slow circuits.

Dielectric Absorption

We begin with dielectric absorption, also known as "soakage" and sometimes as "dielectric hysteresis"—perhaps the least understood and potentially most damaging capacitive effect. Upon discharge, most capacitors are reluctant to give up all of their former charge. Figure 2 illustrates the effect. After being charged to V volts at time t_0, the capacitor is shorted by the switch at time t_1. At time t_2, the capacitor is open-circuited; a residual voltage slowly builds up across its terminals and reaches a nearly constant value. This voltage is due to "dielectric absorption."

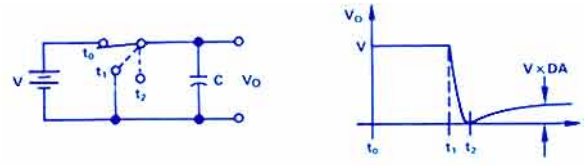


Figure 2. Residual voltage characterizes capacitor dielectric absorption.

Standards techniques for specifying or measuring dielectric absorption are few and far between. Measured results are usually expressed as the percentage of the original charging voltage that reappears across the capacitor. Typically, the capacitor is charged for more than 1 minute, then shorted for an established time between 1 and 10 seconds. The capacitor is then allowed to recover for approximately 1 minute, and the residual voltage is measured (see reference 10).

In practice, dielectric absorption makes itself known in a variety of ways. Perhaps an integrator refuses to reset to zero, a voltage-to-frequency converter exhibits unexpected nonlinearity, or a sample-and-hold exhibits varying errors. This last manifestation can be particularly damaging in a data-acquisition system, where adjacent channels may be at voltages which differ by nearly full scale. Figure 3 illustrates the case in a simple sample-hold.

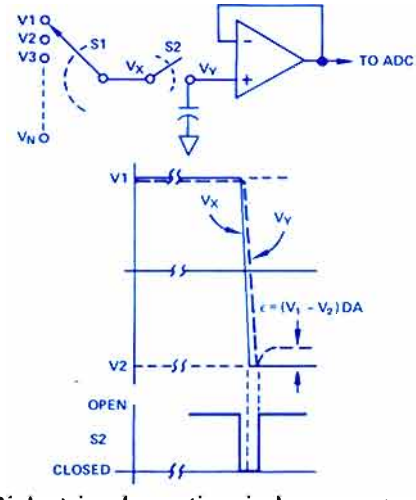


Figure 3. Dielectric absorption induces errors in sample-and-hold application.

The dielectric absorption is a characteristic of the dielectric material itself, although it can be affected by inferior manufacturing processes or electrode materials. As a percentage of the charging voltage, dielectric absorption specifications range from a low of 0.02% for Teflon, polystyrene, and polypropylene capacitors to a high of 10% or more for some aluminum electrolytics. For some time-frames, the D.A. of polystyrene can be as low as 0.002%.

Common ceramic and polycarbonate types display typical dielectric absorptions of 0.2%; this corresponds to one-half of an LSB at only 8 bits! Silver mica, glass, and tantalum capacitors typically exhibit even larger dielectric absorptions, ranging from 1.0% to 5.0%, with those of polyester devices falling in the vicinity of 0.5%. As a rule, if your capacitor's spec sheet does not discuss dielectric absorption *in your time frame and voltage range*, exercise caution.

Dielectric absorption can produce long tails in the transient response of fast-settling circuits, such as those found in high-pass active filters or ac amplifiers. In some devices used for such applications, Figure 1's R_{da}-C_{da} model of dielectric absorption can have a time constant of milliseconds.* In fast-charge, fast-discharge applications, the dielectric absorption resembles "analog memory"; the capacitor tries to remember its previous voltage.

In some designs, you can compensate for the effects of dielectric absorption if it is simple and easily characterized, and you are willing to do custom-tweaking. In an integrator, for instance, the output signal can be fed back through a suitable compensation network, tailored to cancel the circuit equivalent of the dielectric absorption by placing a negative impedance effectively in parallel. Such compensation has been shown to improve sample- and-hold circuit performance by factors of 10 or more (Reference 7).

Parasitics and Dissipation Factor

In Figure 1, a capacitor's leakage resistance, R_p, the effective series resistance, R_s, and effective series inductance, L, act as parasitic elements which can degrade an external circuit's performance. The effects of these elements are often lumped together and defined as a dissipation factor, or DF.

A capacitor's leakage is the small current that flows through the dielectric when a voltage is applied. Although modeled as a simple insulation resistance (R_p) in parallel with the capacitor, the leakage actually is nonlinear with voltage. Manufacturers often specify leakage as a megohm-microfarad product, which describes the dielectric's self-discharge time constant, in seconds. It ranges from a low of 1s or less for high-leakage capacitors, such as aluminum and tantalum devices, to the 100's of seconds for ceramic capacitors. Glass devices exhibit self-discharge time-constants of 1,000 or more; but the best leakage performance is shown by Teflon and the film devices (polystyrene, polypropylene), with time constants exceeding 1,000,000 megohm-microfarads. For such a device, leakage paths—created by surface contamination of the device's case or in the associated wiring or physical assembly—can overshadow the dielectric's leakage.

Effective series inductance, ESL (Figure 1) arises from the inductance of the capacitor leads and plates, which, particularly at the higher frequencies, can turn a capacitor's normally capacitive reactance into an inductive reactance. Its magnitude depends on construction details within the capacitor. Tubular wrapped-foil devices display significantly more lead inductance than molded radial-lead configurations. Multilayer ceramic and film-type devices typically exhibit the lowest series impedances, while tantalum and aluminum electrolytics typically exhibit the highest. Consequently, electrolytic types usually prove insufficient for high-speed local bypassing applications.

Manufacturers of capacitors often specify effective series inductance by means of impedance-versus-frequency plots. These show graphically, and not surprisingly, that the devices display predominantly capacitive reactance at low frequencies, with rising impedance at higher frequencies because of their series inductance.

Effective series resistance, ESR (resistor R_s of Figure 1), is made up of the resistance of the leads and plates. As noted, many manufacturers lump the effects of ESR, ESL, and leakage into a single parameter called *dissipation factor*, or DF. Dissipation factor measures the basic inefficiency of the capacitor. Manufacturers define it as the ratio of the energy lost to energy stored per cycle by the capacitor. The ratio of equivalent series resistance to total capacitive reactance—at a specified frequency—approximates the dissipation factor, which turns out to be equivalent to the reciprocal of the figure of merit, Q.

Dissipation factor often varies as a function of both temperature and frequency. Capacitors with mica and glass dielectrics generally have DF values from 0.03% to 1.0%. For ceramic devices, DF ranges from a low of 0.1% to as high as 2.5% at room temperature. And electrolytics usually exceed even this level. The film capacitors usually are the best, with DF's of less than 0.1%.

Tolerance, Temperature, and Other Effects

In general, precision capacitors are expensive and—even then—not necessarily easy to buy. In fact, choice of capacitance is limited by the the range of available values and tolerances. Tolerances of ± 1% for some ceramics and most film-type devices are common, but with possibly unacceptable delivery times. Most film capacitors can be made available with tolerances of less than ± 1%, but on special order only.

Most capacitors are sensitive to temperature variations. Dissipation factor, dielectric absorption, and capacitance itself are all functions of temperature. For some capacitors, these parameters vary approximately linearly with temperature; in others they vary quite nonlinearly. Although not usually important for sample-and-hold applications, an excessively large temperature coefficient (ppm/°C) can prove harmful to the performance of precision integrators, voltage-to-frequency converters, and oscillators. NPO ceramic capacitors, with temperature-drift as low as 30 ppm/°C, usually do the best. On the other hand, aluminum electrolytics' temperature coefficients can exceed 10,000 ppm/°C.

A capacitor's maximum working temperature should also be considered. Polystyrene capacitors, for instance, melt near 85°C, compared to Teflon's ability to survive temperatures up to 200°C.

Sensitivity of capacitance and dielectric absorption to applied voltage can also hurt capacitor performance in a circuit application. Although capacitor manufacturers do not always clearly specify voltage coefficients, the user should always consider the possible effects of such factors. For instance, when maximum voltages are applied, some high-density ceramic devices can experience a decrease in capacitance of 50% or more!

*Much longer time constants are also quite usual. In fact, some devices can be modeled by several paralleled R_{da}–C_{da} circuits, with a wide range of time constants.

Similarly, the capacitance and dissipation factor of many types vary significantly with frequency, mainly as a result of a variation in dielectric constant. In this regard, the better dielectrics are polystyrene, polypropylene, and Teflon.

Assemble Critical Components Last

The designer's worries don't end with the design process. Commonly used printed-circuit-board assembly techniques can prove ruinous to even the best of designs. For instance, some commonly used p-c board cleaning solvents can infiltrate certain electrolytic capacitors—those with rubber end caps are particularly susceptible. Even worse, some of the film capacitors, polystyrene in particular, actually melt when contacted by some solvents. Rough handling of the leads can damage still other capacitors, creating random or even intermittent circuit problems. Etched-foil types are particularly delicate in this regard. To avoid these difficulties, it may be advisable to mount especially critical components as the last step in the board assembly process—if possible.

Designers should also consider the natural failure mechanisms of capacitors. Metallized film devices, for instance, often self-heal. They initially fail due to conductive bridges that develop through small perforations in the dielectric films. But the resulting fault currents can generate sufficient heat to destroy the bridge, thus returning the capacitor to normal operation (at slightly lower capacitance). Of course, applications in high-impedance circuits may not develop sufficient current to clear the bridge.

Tantalum capacitors also exhibit a degree of self-healing, but—unlike film capacitors—the phenomenon depends on the temperature at the fault location rising slowly. Therefore, tantalum capacitors self-heal best in high impedance circuits which limit the surge in current through the capacitor's defect. Use caution, therefore, when specifying tantalums for high-current applications.

Electrolytic capacitor life often depends on the rate at which capacitor fluids seep through end caps. Epoxy end seals perform better than rubber seals, but an epoxy sealed capacitor can explode under severe reverse-voltage or overvoltage conditions.

RESISTORS AND POTS

Designers have a broad range of resistor technologies to choose from, including carbon composition, carbon film, bulk metal, metal film, and both inductive and non-inductive wire-wound types. As perhaps the most basic—and presumably most trouble-free—of components, the resistor is often overlooked as a potential source of errors in high-performance circuits. Yet, an improperly selected resistor can subvert the accuracy of a 12-bit design by developing errors well in excess of 122 ppm, (½ LSB). When did you last take the time to actually read a resistor data sheet? You'd be surprised at what can be learned from an informed review of the data.

Consider the circuit of Figure 4, which amplifies a 0-to-100-mV input signal 100 times for conversion by a 12-bit ADC with a 0-to-10-volt input range. The gain-setting resistors can be bought in initial tolerances of as low as ±0.001% (10 ppm) in the form of precision bulk metal-film devices. Alternatively, the initial tolerance

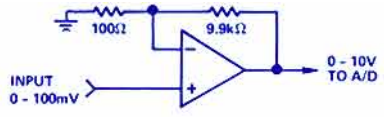


Figure 4. Temperature changes can reduce amplifier accuracy.

of the resistors may be corrected through calibration or selection. Consequently, the initial gain accuracy of the circuit can be set to whatever tolerance is required, limited perhaps by the accuracy of calibration instrumentation.

Temperature changes, however, can limit the accuracy of the amplifier of Figure 4 in several ways. The absolute temperature coefficients of the resistors are unimportant, as long as they track. Even so, carbon composition resistors, with temperature coefficients of approximately 1,500 ppm/°C, would not suit the application. Even if the tempcos could be matched to an unlikely 1%, the resulting 15 ppm/°C differential would prove inadequate—a shift of as little as 8°C would create a ½-LSB error of 120 ppm.

Manufacturers do offer metal film and bulk metal resistors with absolute temperature coefficients ranging between ±1 and ±100 ppm/°C. Beware, though; temperature coefficients can vary a great deal, particularly among resistors from different batches. To avoid this problem, expensive matched resistor pairs are offered by a few manufacturers, with temperature coefficients that track one another to within 2 to 10 ppm/°C. Low-priced thin-film networks are good and are widely used.

Unfortunately, even matched resistor pairs cannot fully solve the problem of temperature-induced resistor errors. Figure 5a illustrates error-inducing through self-heating. The resistors have identical temperature coefficients but dissipate considerably different amounts of power in this circuit. With an assumed thermal resistance (data sheet) of 125°C/W for ¼-watt resistors, resistor R1's temperature rises by 0.0125°C, while resistor R2's temperature rises by 1.24°C. With a temperature coefficient of 50 ppm/°C, the result is an error of 62 ppm (0.006%).

Even worse, the effects of self-heating create nonlinear errors. In the example of Figure 5a, with half the voltage input, the resulting error is only 15 ppm. Figure 5b graphs the resulting nonlinear transfer function for the circuit of Figure 5a. This is by no means a worst-case example; smaller resistors would give even worse results due to their higher thermal resistance.

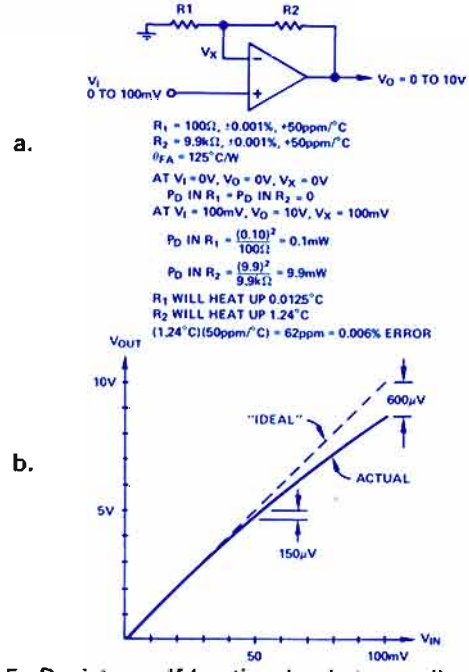


Figure 5. Resistor self-heating leads to nonlinear amplifier response. (a) Anatomy of temperature-induced nonlinearity. (b) Nonlinear transfer function (scale exaggerated).

The use of higher-wattage resistors for those devices that dissipate the greatest power can minimize the effects of resistor self-heating. Alternatively, thin- or thick-film resistor networks minimize the effects of self heating by spreading the heat more evenly over all the resistors in a given package.

Often overlooked as a source of error, the temperature coefficient of resistance of typical wire or pc-board interconnects can add to a circuit's errors. Metals used in p-c boards and for interconnecting wires (e.g., copper) have a temperature coefficient as high as 3,900 ppm/°C. A precision 10-ohm, 10 ppm/°C wirewound resistor, with 0.1-ohms of interconnect resistance, for instance, effectively turns into a 45 ppm/°C resistor. The temperature coefficients of interconnects play a particularly significant role in precision hybrids, where thin-film interconnects have non-negligible resistance.

One final consideration applies mainly to designs that see widely varying ambient temperatures: a phenomenon known as temperature retrace describes the change in resistance which occurs after a specified number of cycles of exposure to low and high ambients with constant internal dissipation. Temperature retrace can exceed 10 ppm, even for some of the better metal-film components.

In summary, to design resistance circuits for minimum temperature-related errors, consider the following (along with their cost):

- Closely match resistance-temperature coefficients.
- Use resistors with low absolute temperature coefficients.
- Use resistors with low thermal resistance (higher power ratings, larger cases).
- Tightly couple matched resistors thermally; (use standard resistance networks or multiple resistors in a single package).
- For large ratios, consider using stepped attenuators.

Resistor Parasitics

Resistors can exhibit significant levels of parasitic inductance or capacitance, especially at high frequencies. Manufacturers often specify these parasitic effects as a reactance error, in % or ppm, based on the ratio of the difference between the impedance magnitude and the dc resistance, to the resistance, at one or more frequencies.

Wirewound resistors are especially susceptible to difficulties. Although resistor manufacturers offer wirewound components in either normal or noninductively wound form, even noninductively wound resistors create headaches for designers. These resistors still appear slightly inductive (of the order of 20 μH) for R values below 10,000 ohms. Noninductively wound resistors that exceed 10,000 ohms actually exhibit about 5 pF of shunt capacitance.

These parasitic effects can raise havoc in dynamic circuit applications. Of particular concern are applications using wirewound resistors with values both greater and less than 10,000 ohms. Here it is not uncommon to see peaking, or even oscillation. These effects become evident at frequencies in the low-kHz range.

Even in low-frequency circuit applications, parasitic effects in wire wound resistors can create difficulties. Exponential settling to 1 ppm takes 20 time constants or more. Parasitics associated with wire wound resistors can increase settling time beyond the length of those time constants significantly.

Unacceptable amounts of parasitic reactance are often found even in resistors that aren't wirewound. For instance, some metal-film types have significant interlead capacitance, which shows up at high frequencies. Carbon resistors do the best at high frequencies.

Thermoelectric Effects

The junction between any two dissimilar metals creates a thermal EMF. In many cases, it can easily produce the dominant error in a precision circuit design. In wire wound resistors, for instance, the resistance wire generates a thermal EMF of 42 microvolts/°C when joined to the leads (A typical lead material is Alloy 180, consisting of 77% copper and 23% nickel). If the resistor's two terminations see the same temperature, the EMFs cancel and no net error results. However, if the resistor is mounted vertically (Figure 6), the top lead-junction is at higher temperature than the bottom junction, since heat dissipated by the resistor rises.

For a temperature difference of as little as 1°C, an error voltage of 42 microvolts results, a level which easily overwhelms the 25-microvolt offsets of typical precision op amps! A horizontally mounted resistor (Figure 6) can resolve the difficulty. Alternatively, some resistor manufacturers offer, on special order, tinned copper leads, which reduce the thermal EMF to 2.5 microvolts/°C.

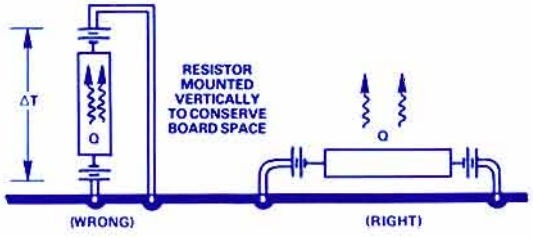


Figure 6. Thermal gradients create significant thermoelectric circuit errors.

In general, designers should strive to avoid thermal gradients on or near critical circuit boards. Often this means thermally isolating components that dissipate significant amounts of power. Thermal turbulence created by large temperature gradients can also result in dynamic noise-like low-frequency errors.

Voltage, Failure, and Aging

Resistors are also plagued by changes as a function of applied voltage. The deposited-oxide high-megohm type components are especially sensitive, with voltage coefficients ranging from 1 ppm/volt to more than 200 ppm/volt. This is another reason to exercise caution in precision applications, such as high-voltage dividers.

Resistors' failure mechanisms can also create circuit difficulties if not carefully considered. Carbon-composition resistors fail safely by turning into open circuits. Consequently, in some applications, these components play a useful secondary role as a fuse. Replacing such a resistor with a carbon-film type can lead to trouble, since carbon-film devices can fail as short circuits. (Metal-film components usually fail as open circuits.)

All resistors tend to change slightly in value with age. Manufacturers specify long-term stability in terms of change—ppm/year. Values of 50 or 75 ppm/year are not uncommon among metal film resistors. For critical applications, metal-film devices should be burned-in for at least one week at rated power. During burn-in, R values can shift by up to 100 or 200 ppm. Metal film resistors may need 4,000 or 5,000 operational hours for full stabilization, especially if they are deprived of a burn-in period.

Resistor Excess Noise

Most designers have some familiarity with thermal, or Johnson, noise in resistors. But a less widely recognized second noise phenomenon, called excess noise, can prove particularly trouble-

some in precision op amp and converter circuits. Excess noise becomes evident only when current passes through a resistor.

To review briefly, thermal noise results from the thermally induced random vibration of charge carriers in a resistor. Although the average current from these vibrations remains zero, instantaneous charge motions result in an instantaneous voltage across the resistor's terminals.

Excess noise, on the other hand, occurs primarily when dc flows in a discontinuous medium, such as a carbon composition resistor. The current flows unevenly through the compressed carbon granules, creating microscopic particle-to-particle "arcing". The phenomenon gives rise to a 1/f noise-power spectrum, in addition to the thermal noise spectrum. In other words, the excess spot noise voltage increases as the inverse square-root of frequency.

Excess noise often surprises the unwary designer. Resistor thermal noise and op amp noise set the noise floor in typical op-amp circuits. Only when voltages appear across input resistors and cause current to flow does the excess noise become a significant—and often dominant—factor. In general, carbon composition resistors generate the most excess noise. As the conductive medium becomes more uniform, excess noise becomes less significant. Carbon film resistors do better, and metal film resistors do better yet.

Manufacturers specify excess noise in terms of a noise index—the number of microvolts of rms noise in the resistor in each decade of frequency per volt of dc drop across the resistor. The index can rise to 10dB (3 microvolts per dc volt per decade of bandwidth) or more. Excess noise is most significant at low frequencies. Above 100 kHz, thermal noise predominates.

Potentiometers

Trim potentiometers can suffer from most of the phenomena that plague fixed resistors. Users must also remain vigilant against additional hazards unique to these components.

For instance, many trim potentiometers are not sealed and can be severely damaged by board-washing solvents, and even by excessive humidity. Vibration—or simply extensive use—can damage resistive-element and wiper terminations. Contact noise, tempcos, parasitic effects, and limitations on adjustable range can all hamper circuit operation. Furthermore, the limited resolution of wirewound types and the hidden limits to resolution in cermet and plastic types (hysteresis, incompatible material tempcos, slack) make the obtaining and maintaining of precise settings anything but an "infinite resolution" process. Rule: Use infinite care and infinitesimal adjustment range to avoid infinite frustration.

PRINTED-CIRCUIT BOARDS

Printed-circuit boards act as "unseen components" in all precision circuit designs. Since designers rarely consider the electrical characteristics of PC boards as additional circuit components, the circuit's performance usually ends up worse than predicted.

Printed-circuit-board effects that are harmful to precision circuit performance include leakage resistances, voltage drops in ground foils, stray capacitances, dielectric absorption and related "hook" (a salient feature of the circuit's step-response waveform). In addition, the tendency of p-c boards to absorb atmospheric moisture ("hygroscopicity") means that changes in humidity often cause the contributions of some parasitic effects to vary from day to day.

In general, printed-circuit-board effects can be divided into two categories—those that most noticeably affect the static or dc operation of the circuit, and those that most noticeably affect dynamic or a-c circuit operation.

Static PC-Board Effects

Leakage resistance is the dominant static circuit board effect. Contamination of the board's surface, in the form of flux residues, deposited salts, and other debris can create leakage paths between circuit nodes. Even on well cleaned boards, it is not unusual to find 10 nA or more of leakage to nearby nodes from 15-volt supply rails.* Nanoamperes of leakage current into the wrong nodes often cause volts of error at a circuit's output; for example, 10 nA into a 10-megohm resistance causes 0.1 V of error.

To identify nodes sensitive to the effects of leakage currents, ask the simple question: If a spurious current of a few nanoamperes or more were injected into this node, would it matter?

If the circuit is already built, you can localize moisture sensitivity to a suspected node with a classic test. While observing the circuit's operation, blow on potential trouble spots through a simple soda straw. The soda straw focuses the breath's moisture, which, with the board's salt content in susceptible portions of the design, disrupts circuit operation upon contact.

There are several means of eliminating simple surface leakage problems. Thorough washing of circuit boards to remove residues helps considerably. A simple procedure includes vigorously brushing the boards with isopropyl alcohol, followed by a thorough washing with deionized water and an 85°C bakeout for a few hours. Be careful when selecting board-washing solvents, though. If cleaned with Freon-based solvents, some water-soluble fluxes create salt deposits, exacerbating the leakage problem.

Unfortunately, if a circuit displays a sensitivity to leakage, even the most rigorous cleaning can offer only a temporary solution. Problems soon return upon exposure to handling, foul atmospheres, and high humidity. *Guarding*, on the other hand, offers a fairly reliable and permanent solution to the problem of surface leakage. Well-placed guards can eliminate leakage problems, even for circuits exposed to harsh industrial environments.

Guarding principles are simple: Surround sensitive nodes with conductors that can readily sink stray currents, and maintain those conductors at the exact potential of the sensitive node. The guard potential must be maintained close to the potential of the sensitive node, otherwise the guard will serve as a source rather than a sink. For example, to keep the leakage current into a node below a picoampere, assuming 1000-megohm leakage resistance, the guard and the node must be within 1.0 millivolts of one another.

Figures 7a and 7b illustrate the guarding principle as applied to typical inverting and non-inverting op-amp applications. Figure 7c illustrates an actual circuit-board layout for a guard. Note that, to be most effective, the guard pattern should appear on both sides of the circuit board. Try to include the guards when first laying out a new board pattern, from the beginning of the layout process. At later stages, there is usually insufficient space left to locate them optimally—if at all.

Dynamic PC-Board Effects

Although static pc board effects can come and go with changes in humidity or board contamination, problems that most noticeably

*Unfortunately, the standard op-amp pinout places the −15V supply pin right next to the + input, which is often hoped to be at high impedance.

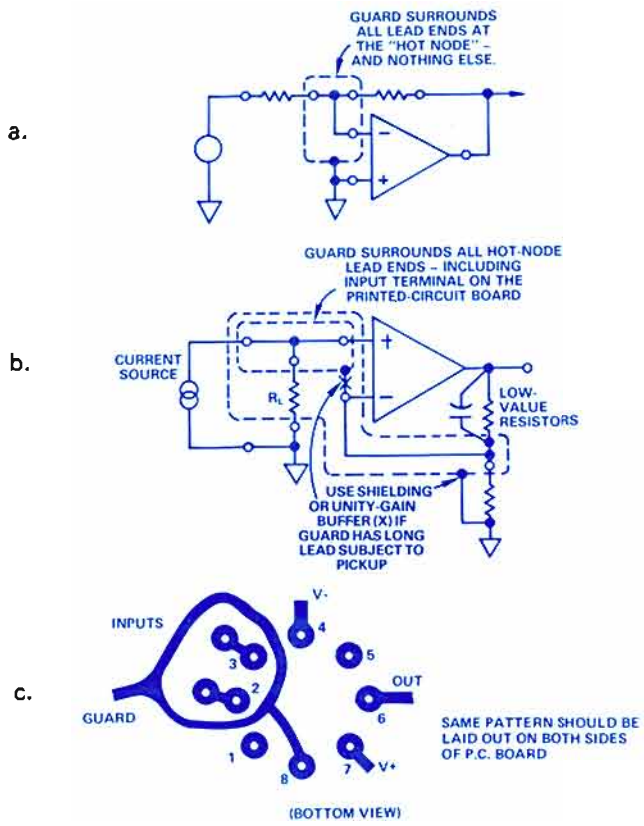


Figure 7. Proper circuit guarding resolves both static and dynamic pc-board induced errors. (a) Use of guard in inverting application. (b) Use of local guard in non-inverting application. Voltage buffer would help in guarding cable. (c) Printed-circuit board guard pattern for op amp.

affect the dynamic performance of a circuit usually remain relatively constant. Short of a new design, they can't be fixed by washing or any other simple fixes. As such, they can permanently and adversely affect a design's specifications and performance.

The problems of stray capacitance, linked to lead and component placement, are reasonably well known to most circuit designers. Since lead placement can be permanently dealt with by correct layout, any remaining difficulty is solved by training assembly personnel to orient components or bend leads in an optimal way.

Dielectric absorption, on the other hand, represents a more troublesome and still poorly understood circuit-board phenomenon. Like dielectric absorption in capacitors, dielectric absorption in a printed-circuit board can be modeled by a series resistor and capacitor connecting two closely spaced nodes (Figure 8). Its effect is inverse with spacing and linear with length. The model's effective capacitance ranges from 0.1 to 2.0 pF, with the resistance ranging from 50 to 500 MΩ. Values of 0.5 pF and 100 MΩ are most common. Consequently, circuit-board dielectric absorption

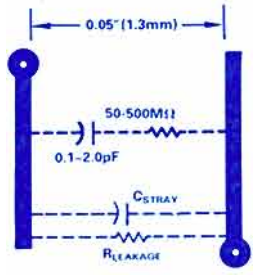


Figure 8. Dielectric absorption plagues dynamic response of pc-based circuits.

interacts the most with high-impedance circuits.

Such dielectric absorption most noticeably influences dynamic circuit response, for example, settling time. Unlike circuit leakage, the effects are not usually linked to humidity or other environmental conditions, but rather, are a function of the board's dielectric properties. The chemistry involved in producing plated-through holes seem to exacerbate the problem. If your circuits do not meet expected transient response specs, you should consider circuit-board dielectric absorption as a possible cause.

Fortunately, there are solutions. As in the case of capacitor dielectric absorption, external components can be used to compensate for the effect. More importantly, surface guards that totally isolate sensitive nodes often completely eliminate the problem (The guards must be duplicated on both sides of the board).

Circuit-board "hook", similar if not identical to dielectric absorption, is characterized by a variation in effective circuit-board capacitance with frequency. In general, it affects the transient response of high-impedance circuits where the board's capacitance is an appreciable portion of the total circuit capacitance. Circuits operating at frequencies below 10 kHz are the most susceptible. As in circuit-board dielectric absorption,the board's chemical makeup very much influences its effects.

DON'T OVERLOOK ANYTHING

Remember, if your precision op-amp or data-converter-based design does not meet specs, try not to overlook anything in your efforts to find the error sources. Analyze both active and passive components, and try to identify and challenge any assumptions or preconceived notions that may blind you to the facts. Take nothing for granted.

For example, when not tied down to prevent motion, cable conductors, moving within their surrounding dielectrics, can create significant static charge buildups that cause errors, especially when connectd to high-impedance circuits. Rigid cables, or even costly low-noise Teflon-insulated cables, are an expensive alternative.

As more high-precision op amps and higher resolution data converters become available, and system designs call for higher speed and accuracy, a thorough understanding of the error sources described in this article becomes more important.

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DIGITAL FIR FILTERS WITHOUT TEARS

Designing and Implementing Non-Recursive Filters for DSP
New Low-Power Multipliers and Multiplier/Accumulators Speed Filter Design

by Bill Windsor and Paul Toldalagi

Digital filters once required specialized design techniques, high-performance costly hardware, and complicated software to implement; for these reasons, they found only restricted application. Today, in sharp contrast, the availability of low-cost high-speed digital signal-processing ICs, such as multipliers and multiplier/accumulators, combined with easy-to-use standardized design procedures, has dramatically simplified filter implementation. Consequently, if your applications require filters with rolloffs in excess of 24 dB/octave, you should include digital filters in your design repertoire.

In these pages, we will compare digital and analog filters, discuss the various digital filter architectures, and—as an example—show you a step-by-step method of designing FIR (non-recursive) filters. A set of references will show you where to find information on topics only touched on lightly here.

COMPARE DIGITAL AND ANALOG FILTERS

Digital filters increasingly find their way into modems, radars, spectrum analyzers, and speech- and image-processing equipment, and for good reasons: Compared to analog filters, digital designs offer sharper rolloffs, require no calibration, and have greater stability with time, temperature, and power-supply variations. Simple software changes can alter a digital filter's response in real time, creating so-called "adaptive filters," whereas analog filters usually require hardware changes.

But digital filters do not satisfy every application. Analog techniques are usually most cost-effective in designs calling for rolloffs of up to about 24 dB/octave. As rolloff requirements exceed 24 to 36 dB/octave, however, digital filters increasingly make more sense. In fact, in applications calling for such steep rolloffs, many designers find digital filters significantly easier to develop. Prototypes can be easily altered through software changes. Also, software simulations of digital filter designs reflect the exact filter performance, whereas computer simulations of analog filters can only approximate true filter performance, since the parameters of analog filters are sensitive to component values that are initially inexact and can vary substantially.

DIGITAL FILTER BASICS

Common digital filter designs fall into two basic categories—non-recursive (finite impulse-response, FIR) and recursive (infinite impulse-response, IIR). Besides straightforward IIR designs, there is a growing interest in types embodying what is known as a lattice topology. But before examining these digital filter types, let us review some digital filter basics.

Digital filters are not as difficult to understand as you might at first think. A previous *Analog Dialogue* article introduced the subject to our readers (Vol. 17, Number 1, 1983, page 3); the references listed at the end of both that article and this one can provide greater detail.

Although filtering is often required for smoothing signals in the time domain, most designers understand the operation of a filter best in the frequency domain. The spectrum of the input signal is multiplied by the frequency response of the filter to produce an output signal with an altered spectrum. This multiplication in the frequency domain is equivalent to convolution of the waveform and a response function in the time domain. What then is convolution?

To understand the process, first consider a transfer function, H(f), with an ideal magnitude graph in the frequency domain as shown in Figure 1a. The function H(f) responds with unity gain to signals having frequency components from 0 Hz to f_1 Hz, where each frequency component is simply a cosine wave at a particular frequency. For instance, the signal, $\cos(2\pi 3t)$, represents a unity-amplitude frequency component at $f = 3$ Hz.

Figure 1b illustrates the spectrum of a signal, X(f), whose time value is $\cos(2\pi f_2 t) + \cos(2\pi f_3 t)$. X(f) therefore represents the sum of two equal components at f_2 and f_3. If you want to extract the f_2 component, leaving behind the f_3 component, you could simply pass the X(f) signal through a low pass filter. In fact, H(f) depicts just such a filter, with a cutoff frequency of f_1. Since H(f) equals 1 at f_2 and 0 at f_3, multiplying H(f) by X(f) gives you $1 \times \cos(2\pi f_2 t) + 0 \times \cos(2\pi f t)$, or simply $\cos(2\pi f_2 t)$.

So far, we have been discussing continuous functions of time. However, in digital filters, we are dealing with sampled data, where a function of time consists of a finite number, k, of discrete values, x(n), per second, where k is the sampling rate and n/k is the discrete variable corresponding to time. Thus, a cosine waveform, in discrete time, is expressed as $\cos(2\pi fn/k)$.

The continuous Fourier transform provides a means for mapping continuous functions of time into the continuous complex frequency domain, and the inverse Fourier transform maps functions of frequency into the time domain. Similarly, the discrete Fourier transformation maps discrete functions of time into the discrete frequency domain, and its inverse transforms discrete functions of frequency into the discrete time domain.

If the function of frequency is the product of two functions—for example, the frequency content of a signal and the transfer function (i.e., the frequency response)—the corresponding time function is the same as the *convolution* of two functions in the time domain—i.e., the signal's time waveform and a time-response function, determined by the transfer function.

Thus, Fourier's theorem, which equates multiplication in the frequency domain to convolution in the time domain, provides a means of calculating the time response directly. As a consequence, the discrete-time convolution:

$$y(n) = [h * x](n) \qquad (1)$$

*See Johnson, Matt, "Implement Stable IIR Filters Using Minimal Hardware," EDN, April 14, 1983, pp. 153-166. Reprint is available from Analog Devices.

is equal to the sum of the products of the signal and the frequency response, i.e.,

$$y(n) = \sum_{m=1}^{N} h(m) \cdot x(n - m) \qquad (2)$$

for all values of n.

Equation 2 represents a series of multiplications and additions, which, if performed in a particular order, will automatically treat the input signal x(n) as if it were put through a low-pass filter. The equation assumes that h(n) is zero for $m < 1$ and for $m > N$, which happens to always be true for FIR filters, where N is the number of samples in h(n).

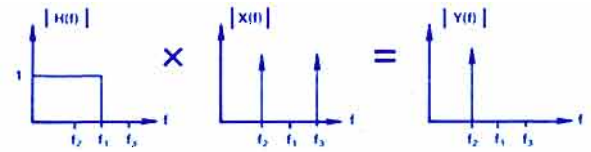

Figure 1. Only one frequency component remains (c) after the filter function (a) multiplies the signal at (b).

To perform the calculation of equation 1, using the Fourier theorem, all you need are the functions h(n) and x(n). These are the inverse discrete Fourier transforms of H(f) and X(f) of Figure 1. The transform of X(f) is a simple cosine wave, $x(n) = \cos(2\pi f_2 n/k) + \cos(2\pi f_3 n/k)$. As discussed in a later section, you can readily calculate the values of x(n) if you know f_2, f_3, and the sample rate, k – the rate at which your analog-to-digital converter is sampling the incoming time-domain signal x(t). You may have a little more difficulty computing the values of h(n), which are called the filter coefficients. But several good computer programs are available to help out, including one from Analog Devices.

To illustrate a practical example of equation 2, consider a 27th order filter, with N = 27. Then, the filter output value y(30), which depends on the 27 preceding values of x, will be:

$$y(30) = h(1) \cdot x(29) + h(2) \cdot x(28) + h(3) \cdot x(27) +$$

$$\ldots + h(26) \cdot x(4) + h(27) \cdot x(3).$$

The physical meaning of this summation is that the filter's step response is synthesized by summing 27 successively delayed versions of the input step, each multiplied by its own coefficient, in effect building an arbitrary step response. For example, if each h(m) is a gain of 1/27, the filter's response to a step will be a 27-step staircase (approximating an analog ramp), followed by constant output; with any input sequence, it performs a 27-interval running average.

The following sections discuss means for calculating the coefficients.

DIGITAL FILTER TYPES

Figure 2 illustrates FIR and two of the most-prominent IIR digital filter topologies, the former straightforward and the latter in the form of a lattice. FIR, or finite impulse response, filters (Figure 2a) have no feedback terms. Their outputs are a function only of a finite number of previous input values (x(n)), and they are by definition nonrecursive. The filter in the example above is an FIR filter. The IIR filters of 2b and 2c will be seen to have recursive terms, in which a value of the output is affected by previous values of the

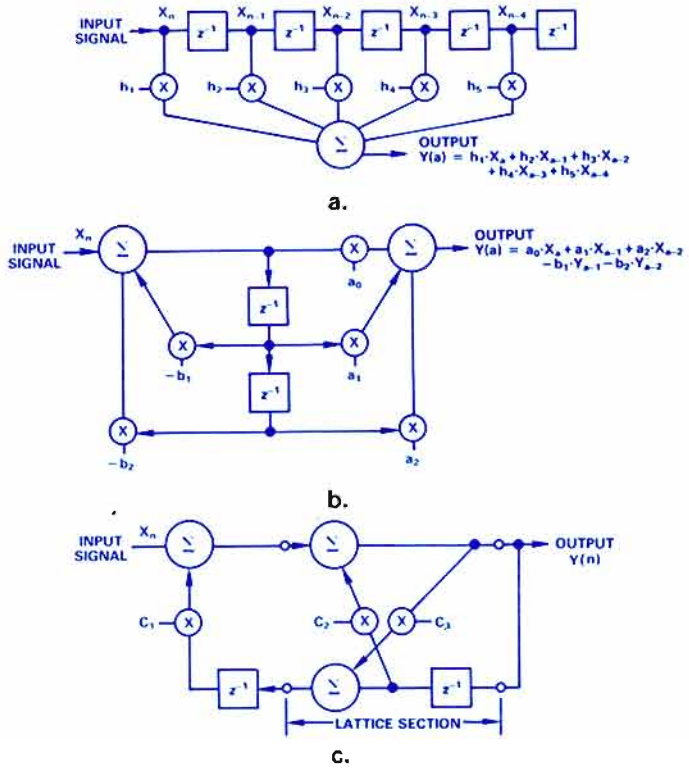

Figure 2. Three common digital filter topologies include FIR (a), IIR (b), and lattice type (c).

output (y(n)), as well as by input values. In comparison to the other types, FIR filters offer:

Stability. FIR filters have no poles in their Z-plane transfer function. Thus, their output is always finite and stable. IIR filters in contrast, require careful design to insure stability. Because FIR designs are based on discrete time delays and have no poles, they can be used to construct filters for which there are no continuous analog equivalents.

Linear Phase Response. You can design FIR filters with linear phase response – the phase delay of the output signal increases linearly with the frequency of the input signal. Linear phase response becomes particularly important in applications such as speech processing, sonar and radar. IIR filters, on the other hand, have nonlinear phase response. Linear phase response is difficult to achieve with continuous analog filters.

Ease of Design. Designers find the FIR filter the easiest of the three forms to understand, design, and implement, especially for indicial response in the time domain.

Low Sensitivity to Coefficient Errors. This permits FIR filters to be implemented with small word sizes – 12-to-16 bits for instance. Typical IIR filters need 16-to-24 bits per coefficient.

Accomodates Adaptive Designs. Adaptive FIR filters are comparatively easy to implement, by changes to the filter coefficients in real time, to adapt the filter's characteristics to external conditions. Adaptive equalization filters in modems, for instance, are programmed to change their characteristics in response to changes in the impedance of the transmission line.

IIR* (infinite impulse response) filter outputs (Figure 2b) combine input values with previous output values, which have been fed back into the circuit. IIR filters are therefore recursive. As in any feedback circuit, to avoid instabilities, IIR filter designs must avoid positive feedback with gains equal to or greater than 1. IIR designs

linear phase shift, and they need large coefficient word sizes to keep rounding errors small and insure stability. Nevertheless, IIR filters have major advantages, including:

Highest Efficiency. IIR designs require fewer filter coefficients, thereby minimizing the number of multiplications and maximizing the throughput.

Least Memory Storage. Because the IIR filter has the least number of coefficients, it requires the least amount of read-only memory (ROM). For example, a typical highpass design requires only four coefficients in an IIR implementation, versus 19 for an FIR equivalent.

Lattice-type digital filters promise greater stability than IIR forms, with less hardware than FIR types. The newest form of digital filter, lattice filters presently have rapidly developing design theory. Although earlier lattice designs were highly sensitive to coefficient accuracy, recent designs have shown less sensitivity to filter parameters than the corresponding IIR filter (by 2 to 3 bits!). A big advantage of lattice filters is that the parameters used in each of the steps can be used for efficient encoding methods, as in linear predictive coding (speech).

DESIGNING FIR FILTERS

Specifications and Tradeoffs

Designers specify non-recursive (i.e., FIR) digital filters similarly to analog filters – a maximum amount of ripple in the passband, a maximum amount of attenuation in the stopband, etc. (See the adjacent definitions of digital filter terminology.) You will need to specify the following design parameters:

N, the number of taps in the filter, which equals the number of filter coefficients

f_p, the passband cutoff frequency

f_s, the stopband cutoff frequency,

$K = (\delta_1/\delta_2)$, the ratio of the ripple in the passband to the ripple in the stopband.

Figure 3 illustrates these parameters for lowpass, highpass and bandpass filters. Designers usually define the units of passband ripple in dB as $20 \log_{10} (1 + \delta_1)$, and the units of stopband ripple, also in dB, as $-20 \log_{10} (\delta_2)$. Passband ripple typically ranges from 0.001 to 1 dB, and stopband ripple from −10 dB to −90 dB. Frequencies f_p and f_s are normalized frequencies, which equal the ratio of the actual signal frequency to the sampling frequency. Consider, for example, a filter designed for a sampling frequency of 100 kHz, a passband cutoff frequency (f_p) of 10 kHz, and a stopband cutoff frequency (f_s) of 20 kHz. Then,

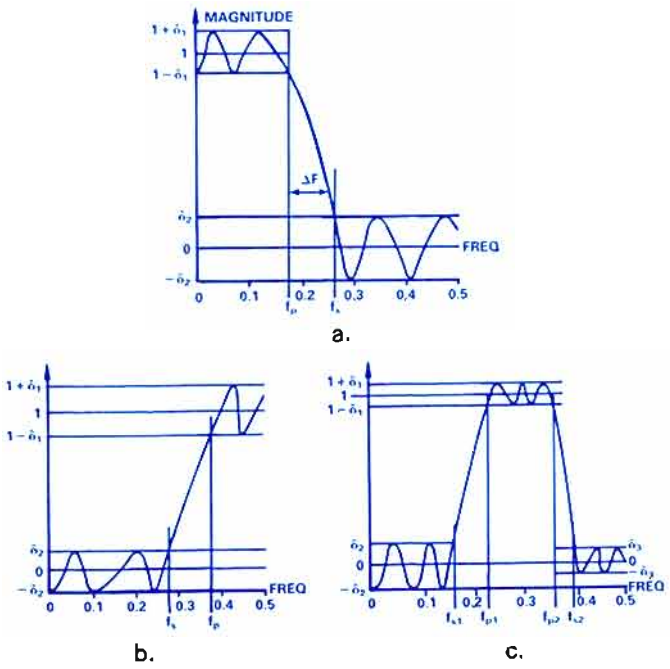

Figure 3. Design parameters defined for lowpass (a), highpass (b), and bandpass (c) filters.

$$f_p \text{ (normalized)} = 10\,\text{kHz}/100\text{kHz} = 0.1$$

$$f_s \text{ (normalized)} = 20\,\text{kHz}/100\text{kHz} = 0.2$$

Note that the normalized frequency axis extends from 0 to only 0.5, since a design in accordance with the Nyquist sampling theorem requires that a signal be sampled at more than twice its highest frequency in order to eliminate the possibility of aliasing.

As always, specifying these design parameters requires some tradeoffs. With a fixed number of filter taps, steeper rolloffs result in greater ripple. For both steep rolloffs and small ripple, you will have to increase the number of filter taps, and therefore the filter's complexity.

Designing FIR Filters Through Windowing

To design a digital filter, you must first calculate the filter's coefficients, h(m), in order to implement equation 2. The two most common design methods include "windowing" and the Remez Exchange algorithm. For almost 95% of design examples, Remez Exchange results in a significantly more efficient filter. The Remez Exchange algorithm has also been coded in Fortran, and is available from Analog Devices, as noted below.

Windowing methods are useful, however, because of their simplicity, and because they also aid in understanding filtering methods, so they are well worth examining. Keep in mind, though, that FIR designs developed through windowing do not perform as well as those obtained through other methods (see Ref. 7, for instance).

Consider the case of an FIR lowpass filter with stopband attenuation greater than 50 dB, normalized passband cutoff frequency (f_p) of 0.2, and normalized stopband cutoff frequency of 0.3. Figure 4 plots the filter's ideal transfer function, H(f). You can obtain the Fourier series coefficients by solving the inverse Fourier transform by equations 3.

$$h(n) = \int_{-0.5}^{0.5} H\left(\epsilon^{j2\pi f}\right) \cdot \epsilon^{j2\pi fn}\, df$$

$$= \int_{-f_1}^{f_1} \epsilon^{j2\pi fn}\, df$$

$$= \int_{-f_1}^{f_1} (\cos 2\pi fn + j \sin 2\pi fn)\, df$$

$$= \frac{\sin(\pi f_1 n)}{\pi n} \qquad (3)$$

Figure 5a shows the resulting set of h(n), which extend to ± infinity. You next multiply the Fourier coefficients by one of several window or weighting functions, as illustrated by Figure 5b and 5c.

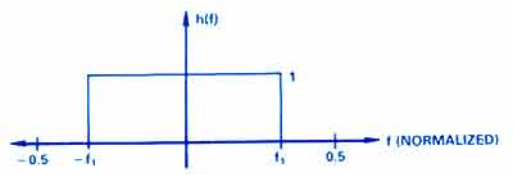

Figure 4. Idealized low-pass filter transfer function

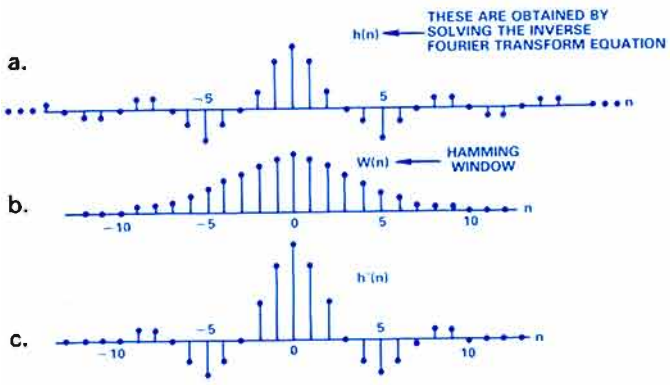

Figure 5. In the window method, a filter's Fourier coefficients (a) multiply a weighting function (b) resulting in (c).

The weighting function is equal to zero above and below some value, ν, which depends on the number of filter taps, N. Multiplying the Fourier coefficients by the weighting function generates a finite impulse response approximation to the desired transfer function, H(f). This guarantees that the Fourier series will converge.

Although several weighting functions will work, Figure 5b plots the widely used Hamming window. Others include the Kaiser, Blackman, and Hanning windows (see Ref. 1). After you choose your window, you can determine the number of coefficients or filter taps, N, from the desired rolloff band, $\Delta f = f_s - f_p$. For the Hamming window, this rolloff bandwidth relates to filter taps, N, by the conservative approximation:

$$\Delta f \approx 4/N \qquad (4)$$

For this design example,

$$\Delta f = f_s - f_p = (0.3 - 0.2) = 0.1.$$

Thus, N = 4/0.1 = 40. This approximation usually yields 2 to 5 more taps than needed, so specify N as 36.

Next, you obtain the filter coefficients, h'(n), of Figure 5c by multiplying each h(n) by the corresponding weighting function w(n) of Figure 5b. Since the coefficients are symmetrical about 0, you need only compute their absolute values (i.e., half the coefficients). The coefficients describe the windowed function, of the form (sin x)/x, which is the Fourier transform of the low pass filter of Figure 4.

Remez Exchange Design

For most FIR applications, the Remez Exchange algorithm offers a more-powerful design technique than the windowing method.* The Remez Exchange algorithm designs an optimal FIR filter as defined by the minimax error criterion (Ref. 7). The minimax criterion specifies a filter that, for a given number of coefficients, *minimizes* the *maximum* ripple in the passband.

*A Fortran-coded version of the algorithm (Refs 2 and 4) is available free of charge by writing to Analog Devices, DSP Marketing, Two Technology Way, Norwood, Massachusetts 02062. Request the "Remez Exchange Application Note."

In general, for a given set of filter specifications, the Remez Exchange algorithm quickly generates an FIR design with the smallest possible number of filter coefficients, particularly in comparison to the results of the windowing method. Also, passband ripples all have equal amplitude, as do all stopband ripples. You designate the ratio, K, of stopband to passband ripple, as noted above.

The Fortran-coded Remez Exchange algorithm is easy to use. Consider, for instance, the case of an FIR low-pass filter with the following specifications:

Sample rate = 50 kHz
f_p (actual) = 10 kHz, f_p (normalized) = 0.2
f_s (actual) = 14 kHz, f_s (normalized) = 0.28
minimum stopband attenuation = 40 dB
maximum passband ripple = 0.2 dB
ripple ratio K = 1 (equal ripple in pass- and stop-bands)

The Fortran program then prompts the user for inputs using five consecutive lines:

Line 1:

FILT = number of filter taps or coefficients. Set this equal to zero if the filter order (number of taps) is not known, as in this design example.

JTYPE = type of filter (set to 1 for low-pass, high-pass, or band-pass filters).

NBANDS = number of pass-bands plus stop-bands in the filter. For a low-pass filter or a high-pass filter as in this example, NBANDS = 2. A band-pass filter has NBANDS = 3.

JPUNCH = (normally set to zero).

LGRID = number of frequency points used in the Remez Exchange algorithm. For most applications, such as in this example, LGRID = 16 suffices. For high-performance filters with more than 50 taps, set LGRID to 32.

Line 2:

Line 2 contains the normalized frequencies of the pass-band and stop-band edges. The number of values here equals twice the number of bands. For the case of the low-pass filter specified above, the pass-band ranges from 0.0 to 0.2 in normalized frequency, and the stop-band edge spans 0.28 to 0.5 in normalized frequency. Line 2 therefore carries these four numbers for this design example.

Line 3:

Line 3 specifies the magnitude of the desired transfer function, V_{out}/V_{in}, in each band. In this example, the low-pass filter has unity gain in the pass-band, and zero gain in the stop-band, so Line 3 contains the numbers 1, 0.

Line 4:

Line 4 specifies the desired relative weights of the two bands. For this example, specify stop-band ripple equal to pass-band ripple, denoted by a 1, 1 on Line 4.

Line 5:

You need Line 5 only if the number of filter taps needed is unknown – as in this example (NFILT = 0). This line specifies the

desired pass-band and stop-band ripple in dB. The program then estimates the number of required filter taps NFILT. Assume in this case that passband ripple does not exceed 0.2 dB, and that stop-band attenuation is 40.0 dB. Line 5 therefore includes the numbers 0.2 and 40.0.

With these inputs, the Fortran program estimates the filter order (number of taps) by approximating design relationships between the filter parameters (Refs. 5 and 6). The result usually falls within four taps of the correct number needed.

Figure 6 illustrates a typical computer result. The "filter length," determined by approximation as noted above, equals 24 taps. The "impulse response" gives the filter coefficients, and the next few lines of Figure 6 simply repeat the program input values for band 1, the pass-band, and band 2, the stop-band. The "desired value" indicates the desired filter transfer functions in the pass- and stop-bands. The "weighting" of the ripples is 1.00 in the passband and 1.00 in the stopband. The "deviation" is the ripple in each band, which equals 0.011 in the passband and 0.011 in the stopband. The "deviation in dB" represents the decibel value of the "deviation" numbers. "Extremal frequencies" denotes frequencies at which maximum passband and stopband ripple occurs.

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                FINITE IMPULSE RESPONSE (FIR)
                LINEAR PHASE DIGITAL FILTER DESIGN
                REMEZ EXCHANGE ALGORITHM

                BANDPASS FILTER

          FILTER LENGTH =  24

          FILTER LENGTH DETERMINED BY APPROXIMATION

          ***** IMPULSE RESPONSE *****
               H(  1) = -0.10748326E-01 = H(  24)
               H(  2) = -0.18704087E-02 = H(  23)
               H(  3) =  0.15714122E-01 = H(  22)
               H(  4) =  0.47213142E-02 = H(  21)
               H(  5) = -0.25240039E-01 = H(  20)
               H(  6) = -0.13135824E-01 = H(  19)
               H(  7) =  0.41533310E-01 = H(  18)
               H(  8) =  0.28864330E-01 = H(  17)
               H(  9) = -0.69702514E-01 = H(  16)
               H( 10) = -0.71426094E-01 = H(  15)
               H( 11) =  0.16081354E+00 = H(  14)
               H( 12) =  0.43491969E+00 = H(  13)

                    BAND  1          BAND  2          BAND
LOWER BAND EDGE     0.000000000      0.280000001
UPPER BAND EDGE     0.200000003      0.500000000
DESIRED VALUE       1.000000000      0.000000000
WEIGHTING           1.000000000      1.000000000
DEVIATION           0.011113827      0.011113827
DEVIATION IN DB     0.193075284    -39.082729340

EXTREMAL FREQUENCIES
   0.0000000   0.0416667   0.0807292   0.1197916   0.1562500
   0.1875001   0.2000000   0.2800000   0.2930208   0.3216665
   0.3607289   0.3997912   0.4414577

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Figure 6. Remez Exchange program output with NFILT initially = 0.

This initial computer run, with N = 24, results in passband ripple of 0.19 dB, and stopband attenuation of 39.08 dB, which do not meet the design specifications. Repeating the computer run, with successively higher values for N, leads to the acceptable results of Figure 7, for N equal to 27.

Hardware Design

Once fully defined, your filter can be readily implemented in hardware. Figure 8 is a functional diagram of a system implementing the 27-tap filter defined above, assuming 16-bit words. The tradeoffs in selecting word size will be discussed later.

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                FINITE IMPULSE RESPONSE (FIR)
                LINEAR PHASE DIGITAL FILTER DESIGN
                REMEZ EXCHANGE ALGORITHM

                BANDPASS FILTER

          FILTER LENGTH =  27

          ***** IMPULSE RESPONSE *****
               H(  1) =  0.37293066E-02 = H(  27)
               H(  2) = -0.72368127E-02 = H(  26)
               H(  3) = -0.90835225E-02 = H(  25)
               H(  4) =  0.77674030E-02 = H(  24)
               H(  5) =  0.15654538E-01 = H(  23)
               H(  6) = -0.11497792E-01 = H(  22)
               H(  7) = -0.28403830E-01 = H(  21)
               H(  8) =  0.14617096E-01 = H(  20)
               H(  9) =  0.50319906E-01 = H(  19)
               H( 10) = -0.17289791E-01 = H(  18)
               H( 11) = -0.97608425E-01 = H(  17)
               H( 12) =  0.19059505E-01 = H(  16)
               H( 13) =  0.31539205E+00 = H(  15)
               H( 14) =  0.48032677E+00 = H(  14)

                    BAND  1          BAND  2          BAND
LOWER BAND EDGE     0.000000000      0.280000001
UPPER BAND EDGE     0.200000003      0.500000000
DESIRED VALUE       1.000000000      0.000000000
WEIGHTING           1.000000000      1.000000000
DEVIATION           0.008834021      0.008834021
DEVIATION IN DB     0.153466403    -41.076831818

EXTREMAL FREQUENCIES
   0.0000000   0.0446429   0.0848214   0.1250000   0.1607143
   0.1875001   0.2000000   0.2800000   0.2911607   0.3179463
   0.3514283   0.3871424   0.4250887   0.4630350   0.5000000

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Figure 7. Remez Exchange program output, N = 27 taps.

The anti-aliasing filter of Figure 8 minimizes high-frequency signal and noise components reaching the a/d converter. In many cases, anti-aliasing filters require rolloffs no greater than 6-24 dB/octave. The a/d converter samples the incoming analog signal at a rate equal to about three times the highest input frequency. Although the Nyquist criterion specifies a sampling rate of at least two times the highest frequency, conservative design practice dictates a factor of three. The RAM stores the a/d converter's output. With a 27-tap filter, you will need 27 RAM locations, each 16-bits wide.

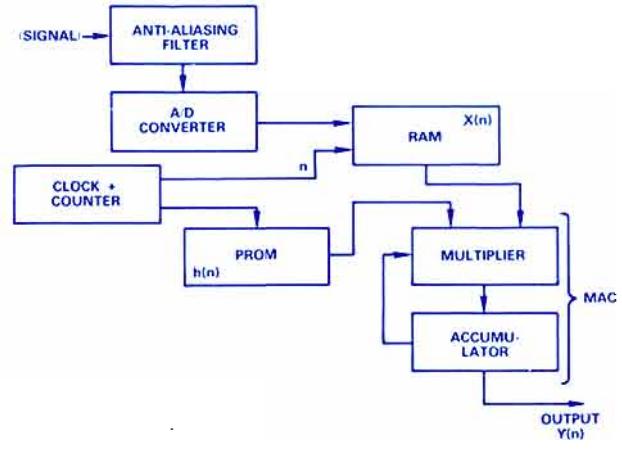

Figure 8. Digital FIR filter system functional block diagram.

A PROM stores the filter coefficients determined earlier. You may need RAM, instead of a PROM, particularly if you wish to implement an adaptive filter. The number of PROM locations equals the number of *different* filter coefficients. Because of symmetry, an FIR filter has N/2 different coefficients for N even (N is the number of taps), and (1 + N)/2 coefficients for N odd. A 27-tap filter therefore requires a PROM with 14 16-bit locations.

The clock and counter step through the RAM and PROM, presenting coefficients and input values to the multiplier. The multiplier/

accumulator combination performs the multiplication and addition as specified by equation 2, and thus forms the heart of the digital filter.

Analog Devices offers a variety of multiplier/accumulator ICs which considerably simplify such digital filter implementations. The ADSP-1010*, for instance, multiplies two 16-bit numbers and accumulates the products in a 35-bit accumulator, which includes 3 bits of extended precision to accomodate overflows resulting from the addition of two or more 32-bit products.

Hardware Details

As a first step in implementing a detailed design, convert the filter coefficients to 16-bit fixed-point or block-floating point numbers. In fixed-point arithmetic, for instance, simply multiply the coefficients by 2^{15}.

Next, round off the coefficients to the nearest least-significant bit. Do not simply truncate the coefficients, since truncation destroys the accuracy of the filter coefficients, whereas rounding achieves performance close to the theoretical limits imposed by your word length. Store the rounded 16-bit coefficients in PROM.

You also must determine whether a standard μP can implement the filter, or whether you will need a dedicated high-speed multiplier IC. To determine the required computational speed, multiply the sampling rate by the number of filter coefficients.

In the above example, a sampling rate of 50 kHz and a filter with 27 taps requires (50kHz × 27) = 1.35 million 16-bit multiply-and-accumulate operations per second, or 740 nanoseconds per combined operation. Few microprocessors can handle such requirements; for instance, the 12.5-MHz version of the Motorola 68000 performs a 16-bit multiplication in 5.6 μs. The Analog Devices ADSP-1010 multiplier/accumulator (MAC), however, readily performs a multiply-and-accumulate operation in only 165 nanoseconds, at low cost and with low power consumption.

To ensure proper multiplications, the memory-control circuitry (RAM, PROM, counter) must retrieve the correct combination of words from memory. The stack and pointers of Figure 9 illustrate one method. Pointer 2 directs the storage of each new data point into RAM. For each new sample, the system computes the transformation by incrementing down from pointer 1 and up from pointer 3 as follows:

$$h(4)\cdot x(n-3) + h(3)\cdot x(n-2) + h(2)\cdot x(n-1) + h(1)\cdot x(n) + h(6)\cdot x(n-5) + h(5)\cdot x(n-4).$$

After computing each sample, pointers 2 and 3 increment; the pointers reset when they reach the stack boundary. Figure 9b details the operation.

Next, decide how to handle accumulator overflow. When a filter performs its multiply-and-accumulate operations, the number of bits in the accumulator will certainly exceed the 32-bit resolution of a single 16 × 16-bit multiplication. To handle overflow, first calculate a reasonable upper bound for the amount of overflow your filter could experience. By summing the squares of the filter coefficients, you can estimate a reasonable level of overflow. Compare this number to the maximum the accumulator can handle.

You can handle accumulator overflow in one of several ways. The ADSP-1010 MAC provides three additional bits of accumulator

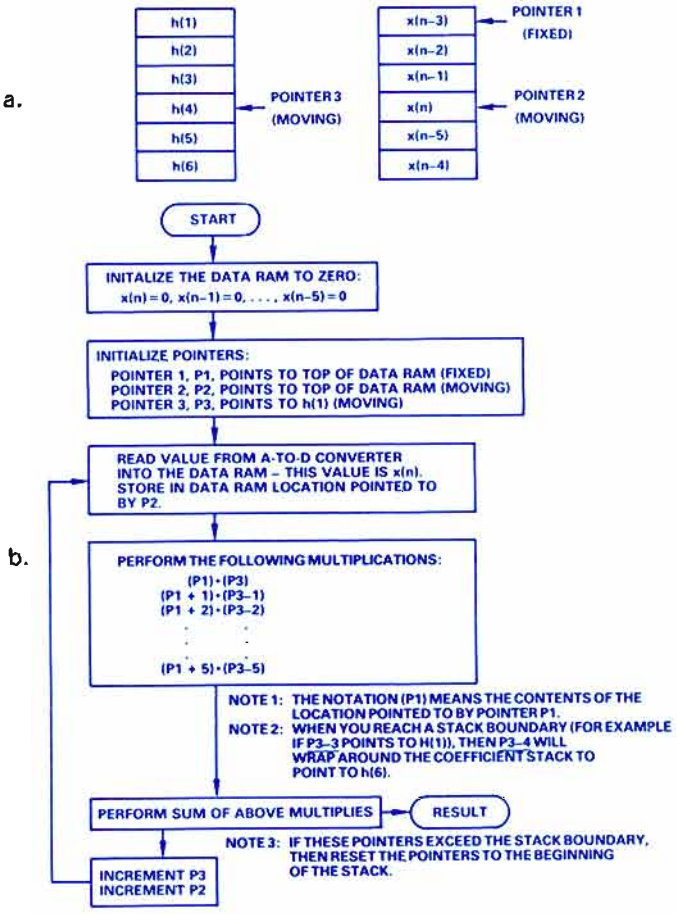

Figure 9. Filter uses pointers (a) to compute convolution as outlined in (b).

precision in addition to the 32 bits needed to handle a single 16 × 16-bit multiplication. This suffices for most applications.

Alternatively, you can scale down the coefficients, from 1 to 5 bits, at the sacrifice of some accuracy. To scale them down, divide them by 2 and apply the overflow test described above. Continue the process until the scaled coefficients pass the overflow test.

Finally, for some applications, you may not want to accomodate the full dynamic range of the input signal. Therefore, just let the accumulator saturate at its maximum value.

Occasionally, required multiply/accumulate speeds exceed the capabilities of even the fastest MAC ICs. In that case, you can combine two or more processors in parallel to increase the throughput. The circuit of Figure 10 combines two ADSP-1010 MACs operating in parallel, thus cutting the multiply/accumulate time per computed point to 75 nanoseconds, which is one-half the normal 150 nanoseconds for a single such component.

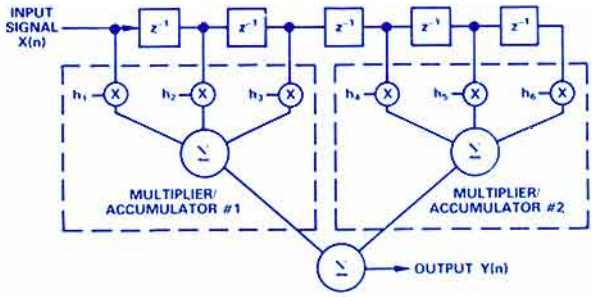

Figure 10. Paralleling two multiplier/accumulators doubles throughput.

*For technical data, use the reply card.

Avoid Rounding and Roundoff Errors

Most digital filter hardware errors result from two sources – rounding and roundoff. *Rounding* errors result from the rounding of filter coefficients, such as those generated in Figures 6 and 7, by a high precision mainframe computer, to the 16-bits of typical digital filter hardware implementations. As noted earlier, rounding produces less error than truncating, but error nonetheless.

Roundoff errors result from consecutive finite precision multiply-and-accumulates. Roundoff errors are more significant than rounding errors, particularly in high-order filters.

Estimating the required word size to avoid such errors can prove tricky. Generally, if your design calls for more than 67 dB of stop-band attenuation or less than 0.05 dB of passband ripple, 16-bit words may lead to excessive errors. Such cases may require 24, and sometimes even 32-bit, word lengths. Software simulation, discussed in a following section, can help you determine word-length requirements before you commit your design to hardware.

To illustrate the significance of these errors, Figure 11 compares simulated performance of 16-bit fixed-point and 32-bit floating-point 27-tap low pass filters. Although the errors appear slight in this case, a similar comparison in Figure 12 for a 90-tap filter shows dramatic differences. For more than 80 dB of stop-band attenuation with 90 taps, more than 16 bits of precision are needed.

Software Simulations

The flow chart of Figure 13 shows a typical software program for simulating the performance of your digital filter with a high-resolution computer. You can obtain from Analog Devices a Fortran-

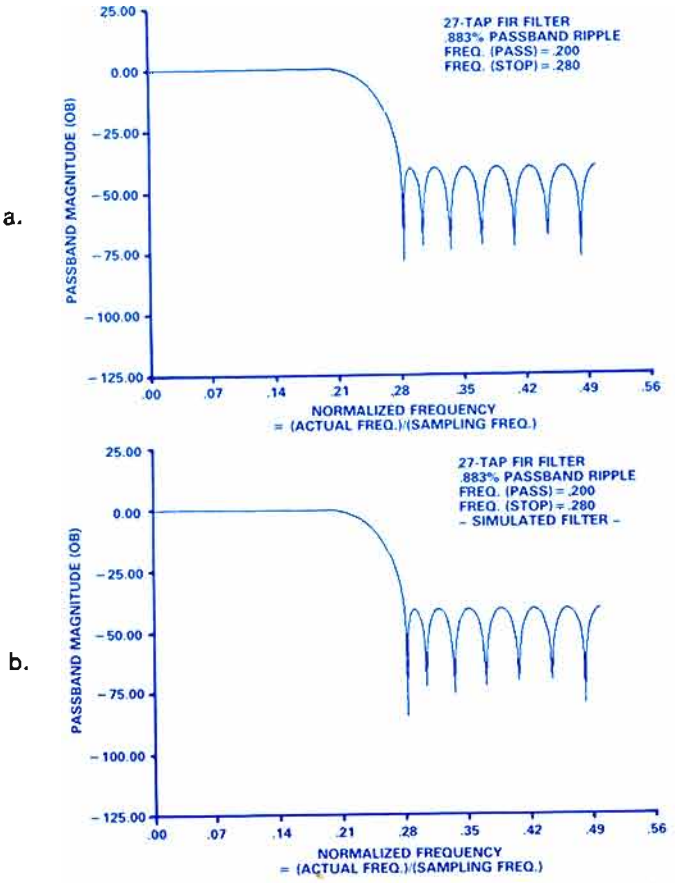

Figure 11. Computer-simulated response of a 27-tap low pass FIR filter using 32-bit arithmetic (a), and 16-bit arithmetic (b).

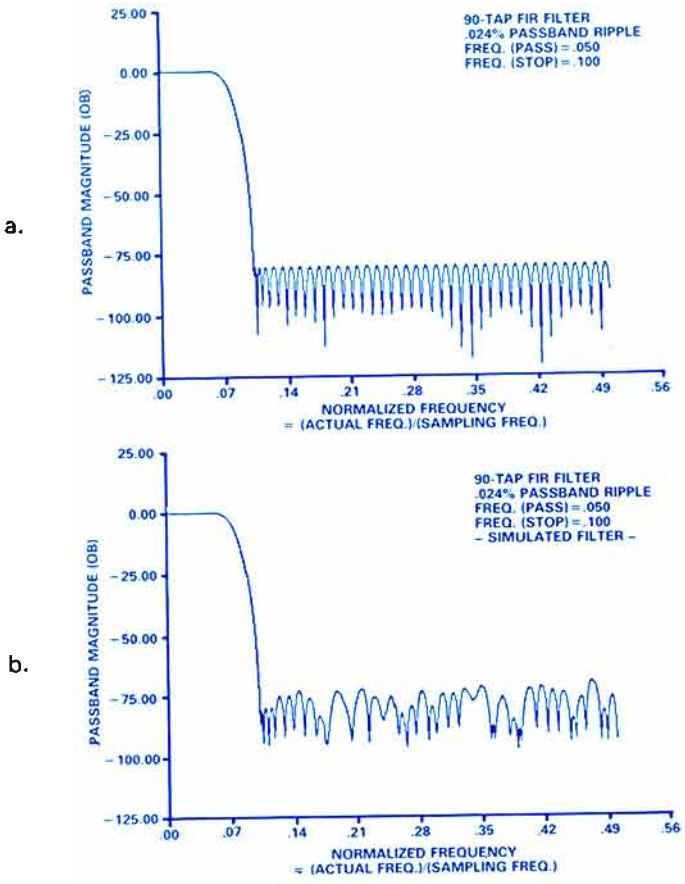

Figure 12. Computer simulated response of a 90-tap low pass FIR filter using 32-bit arithmetic (a), and 16-bit arithmetic (b).

coded version of this program for simulating 16-bit FIR designs, employing the ADSP-1010 16 × 16-bit multiplier/accumulator. It is available from the DSP Marketing Group, under the name, "FIR 16-bit simulation program."

The simulation repeats the steps in the hardware design process. It begins by obtaining the filter coefficients h(n) from the Remez-Exchange computer program, checks for overflow and scales the coefficients, and obtains the 16-bit fixed-point or floating-point coefficients, normally stored in PROM.

The program next simulates a digitized input signal array, x(n), which corresponds to the output of the A/D converter, normally stored in RAM. The number of values in the array equals the number of filter taps. Normally, you should begin the simulation with a cosine wave of frequency 0 Hz, and work you way up to higher frequencies.

The arithmetic operations of the multiplier/accumulator combination are readily simulated. The simulation program restricts the computer's word size to correspond to the limited precision (16 bits) of your filter's hardware implementation. In Fortran, for example, the INTEGER*2 or INTEGER*4 variable type declarations handle this for you.

The simulation program also includes an accumulator overflow check to verify the effectiveness of the initial coefficient scaling operation. If the computer flags an accumulator overflow, you'll have to scale down the coefficients again and re-run the simulation.

The program next computes the filter output values, y(n), by setting up a loop to calculate the transformation of equation 2. For

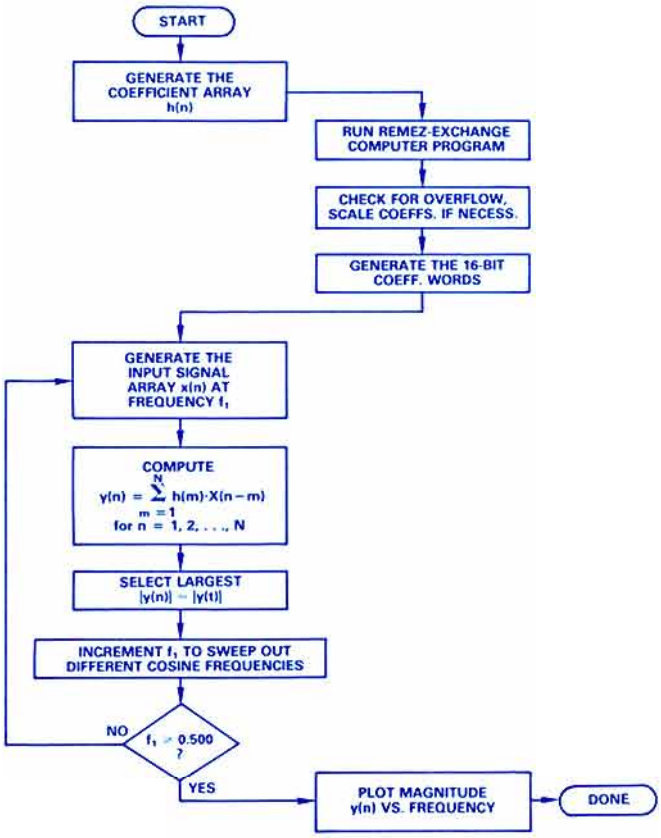

Figure 13. FIR filter simulation program flowchart.

each cosine input, the program computes N values of y(n), where N is the number of filter taps.

The program next finds the magnitude of the filter's output (and therefore the magnitude of the filter's transfer function at that frequency), by choosing the largest absolute value from the y(n) array. This usually comes very close to the actual magnitude of y(n). But if you need better accuracy, you can pass the N points of the y(n) signal through a curve-fitting algorithm which generates a continuous-time signal, y(t).

Once the program computes the output for a cosine wave of 0 Hz, it can calculate outputs for a range of frequencies. You usually want it to sweep from 0 Hz to just below the Nyquist frequency of 0.5 (normalized), in normalized-frequency increments of 0.001. The resulting plot simulates your filter's transfer function. If the plot meets your expectations, you can proceed with the construction of the hardware.

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FOR FURTHER READING

Analog Dialogue, Volume 17, Number 1 (1983) carried a review article summarizing the uses of multiplier/accumulator ICs in a variety of DSP applications. Analog Devices has also collected a recently published series of 5 articles comprising cookbook designs applying DSP to various common filtering, and control applications. If you would like reprints of this set of articles, use the reply card; ask for "EDN series."

Ted Dintersmith, and Paul Toldalagi, "Apply Modern Control Theory to Optimize Digital Systems," *EDN*, April 28, 1983, pp. 165-179.

Matt Johnson, "Implement Stable IIR Filters Using Minimal Hardware," *EDN*, April 14, 1983, pp. 153-166.

John Oxaal, "Temporal Averaging Techniques Reduce Image Noise," *EDN*, March 17, 1983, pp. 211-215.

John Oxaal, "DSP Hardware Improves Multiband Filters," *EDN*, March 31, 1983, pp. 193-197.

Bill Windsor, and Paul Toldalagi, "Simplify FIR-Filter Design With a Cookbook Approach," *EDN*, March 3, 1983, pp. 119-128.

REFERENCES

The following publications should prove useful to the reader seeking even more information on digital signal processing. These publications are *not* available from Analog Devices.

1. Frederick J. Harris, "On the Use of Windows for Harmonic Analysis With the Discrete Fourier Transform," *Proceedings of the IEEE*, Vol. 66, No. 1, January, 1978.

2. J. H. McClellan, T. W. Parks, and L. R. Rabiner, "A Computer Program for Designing Optimum FIR Linear Phase Digital Filters," *IEEE Transactions on Audio and Electroacoustics*, Vol. AU-21, No. 6, December, 1973.

3. A. V. Oppenheim, and R. W. Schafer, *Digital Signal Processing*, (Englewood Cliffs, New Jersey: Prentice-Hall, 1975), chapter 9.

4. A. Peled, and B. Liu, *Digital Signal Processing*, (New York, New York: John Wiley and Sons, Inc., 1976), chapter 2.

5. L. R. Rabiner, "Practical Design Rules for Optimum Finite Impulse Response Low-Pass Digital Filters," *The Bell System Technical Journal*, Vol. 52, No. 6, July-August, 1973.

6. L. R. Rabiner, "Approximate Design Relationships for Low-Pass FIR Digital Filters," *IEEE Transactions on Audio and Electroacoustics*, Vol. AU-21, No. 5, October, 1973.

7. L. R. Rabiner, and B. Gold, *Theory and Application of Digital Signal Processing*, (Englewood Cliffs, New Jersey: Prentice-Hall, 1975), chapter 3.

FILTER TERMINOLOGY

Attenuation – A decrease in output signal magnitude relative to input signal magnitude.

Cutoff frequency – The frequency at which the filter's response drops below the specified pass-band ripple ($1-\delta_1$).

Pass-band – The filter frequency range through which signals pass without more than a specified amount of attenuation.

Stop-band – The filter frequency range through which signals experience a specified degree of attenuation.

Stop-band attenuation – The minimum amount of attenuation in the stop-band.

Pass-band ripple – The maximum deviation from the desired output magnitude in the pass-band.

Sampling rate – The rate at which the system samples the input signal.

Filter coefficients – Numbers representing the inverse Fourier transform of the filter's transfer function. Coefficients define the filter's characteristics and form the basis of digital filter implementations.

Taps – Taps equal the number of sampled input values processed by the filter for each output point. Taps also equals the number of filter coefficients, and can represent a measure of the filter delay.

MONOLITHIC V/F CONVERTER WITH 1-MHz FULL SCALE OUTPUT

AD650 Has 50-ppm Nonlinearity for 100 kHz F.S., 0.1% max for 1 MHz F.S. Accepts Unipolar or Bipolar Signals, Also Converts from Frequency to Voltage

by Larry DeVito

The AD650* is a new high-performance voltage-to-frequency converter (VFC) on a single chip, packaged in a 14-pin plastic or CERDIP dual in-line package. As a VFC, it provides a train of fixed-width output pulses at a frequency proportional to an input voltage or current. For voltage inputs, frequency is scaled by the choice of an external resistance and capacitance, up to a maximum of 1 MHz full-scale. Low-cost, compact, high-resolution V/f converters, such as the AD650, are useful in instrument and system design for such applications as data conversion, signal isolation, and phase-locked loops.

To use the AD650 as a voltmeter, simply apply the voltage to be measured to its input and measure the frequency by counting output pulses during a gate interval. Increase resolution by lengthening the gate interval. The ultimate resolution is limited only by drift and noise.

The AD650 has features not found in other VFCs—for example, offset trimming for the integrator op amp, an available half-scale offset current for applications with bipolar input voltages, and separate analog and digital grounds for minimizing interference between the low-level analog input circuitry and the high-level fast edges associated with digital circuitry.

AD650 vs. AD537 and ADVFC32: The AD650 is the highest-performance monolithic VFC available, featuring guaranteed linearity to within 0.005% at 100kHz full scale, and 0.1% at 1-MHz full-scale. Where linearity and high-speed at high-resolution are not paramount considerations, other alternatives exist:

- For example, the popular AD537* (*Analog Dialogue* 10-2), with maximum nonlinearity of 0.1% at 100kHz and 0.07% at 10kHz, has the convenience of single-supply operation and very low supply current, making it an ideal choice for remote and portable battery-powered applications; it also has a symmetrical square-wave output, independent of frequency, which permits bounceless ac coupling; and it is available in a hermetic TO-100 can, as well as in DIP form.
- The ADVFC32* is available for general-purpose VFC applications calling for maximum nonlinearity of 0.05% at 100kHz and 0.01% at 10kHz; users may also have the comfort of knowing that second sources of this product exist, for applications requiring them.

Prices of these devices in 100s start from: AD650(JN), $7.95; AD537(JH), $5.30; ADVFC32(KN), $5.95.

HOW IT WORKS

The AD650 is a *charge-balance* voltage-to-frequency converter. The input signal current is exactly balanced by an internal feedback current. The feedback is applied as short, precisely controlled bursts of current—i.e., packets of charge. The required number of charge packets, each producing one pulse of the output frequency, is proportional to the input signal level. Figures 1 and 2 show how this is done.

The AD650 (Figure 1) consists of an operational amplifier, a comparator, and a one-shot multivibrator—with period determined by an external capacitor—which controls the locus of flow of a nominally 1-mA precision current. There is also a pin-programmable 0.5-mA bipolar-offset current source. The frequency output is furnished via an open-collector transistor.

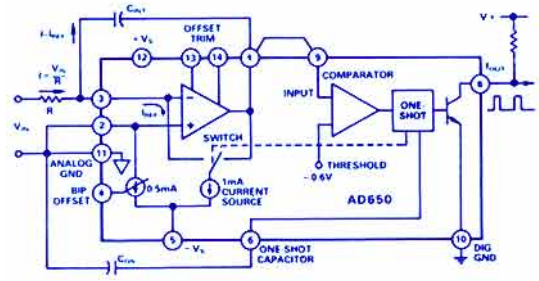


Figure 1. Functional diagram of the AD650, connected for positive input signal.

When the signal circuitry is connected as shown, the positive input voltage develops a current I ($= V_{in}/R$) in the input resistor, flowing continuously through the integrating capacitor, C_{int}, developing a negative-going voltage at the input of the comparator (Figure 2). When the voltage is more negative than $-0.6V$, the comparator flips, triggering the one-shot, which switches the 1-mA current source (I_{ref}) onto the summing point. A current of $(-I_{ref} + V_{in}/R)$ now flows through the capacitor, ramping the output positively for the one-shot's *on* interval, T_{os}. At the end of that period, I_{ref} is switched off the summing point (to the amplifier output, actually, to minimize glitches), and the current is once again V_{in}/R.

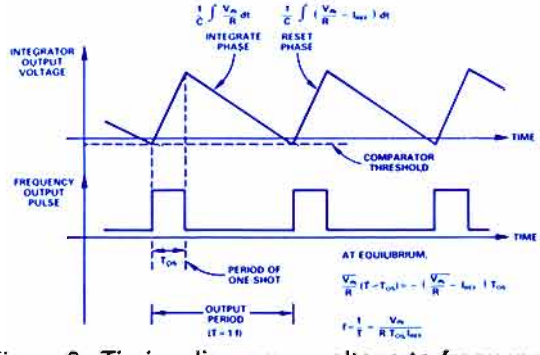


Figure 2. Timing diagram—voltage-to-frequency.

At equilibrium, when the incremental charges, $\Delta Q = I_{ave}\,\Delta t$, are in balance,

$$(I_{ref} - V_{inave}/R)\,T_{os} = (V_{inave}/R)\,(T - T_{os}) \qquad (1)$$

where T is the period, 1/f. Therefore,

$$f = V_{inave}/(RI_{ref} \cdot T_{os}) \qquad (2)$$

It is easy to see that as V_{in} increases, the negative slope increases, triggering the comparator sooner, causing a new cycle sooner, hence an increase in frequency. Note that frequency is independent of the value of C_{int}, depending only on R, the internally generated 1 mA, and the fixed interval, T_{os}, which is established by the external one-shot capacitor.

Since frequency depends directly on R and C_{os}, high-quality com-

ponents with low temperature coefficients should be used. Though not critical, C_{int} affects the sawtooth amplitude, so it is chosen as a function of frequency: $10^{-4}/f_{FS}$ for frequencies below 100kHz, 1000pF for higher frequencies. Apart from these external influences, key factors for the linearity and stability of the AD650 are the amplifier and comparator input stages and the internal precision currents and thresholds, which are set by a buried-Zener reference. Because of its innovative design and simple processing requirements, the AD650 is quite competitively priced.

APPLICATIONS

Factors which make the AD650 easy to use include its open-collector transistor output, which interfaces to any logic family with a simple external pull-up resistor to the logic supply (up to 36 volts above ground). The frequency output has a separate ground, a necessity for minimizing the effects of interference noise so that the excellent linearity of the device can be fully realized.

A set of proper supply bypassing and ground return connections are shown in Figure 3. The analog and digital grounds must be nominally at the same potential, but as much as hundreds of millivolts of noise on the digital ground will be tolerated without compromising the integrity of the analog ground. The 510-ohm pullup resistor shown provides fast rising edges for clean pulses at 1 MHz; higher resistance values can be used at lower frequencies.

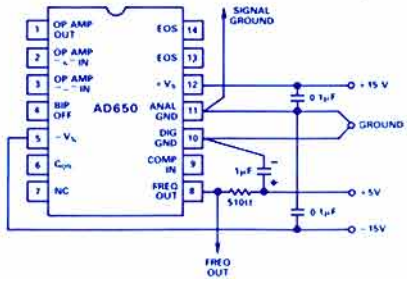


Figure 3. DIP supply connections and bypassing.

Figure 4 shows how the internal bipolar offset current source is used to provide a half-scale offset for a ±10-volt input signal, while providing a 100-kHz output frequency span. The nominally 0.5-mA (±10%) offset current source is enabled when a 1.24kΩ resistor is connected between pins 4 and 5; the offset current is drawn through the non-inverting input terminal of the integrating op amp. Thus, with the grounded 20 kΩ nominal resistance shown, a −10-volt offset is developed at pin 2. Since pin 3 must also be at −10 volts, the current range through R is 20 V/80 kΩ = +0.25 mA at V_{in} = +10 V, and 0 mA at V_{in} = −10 V.

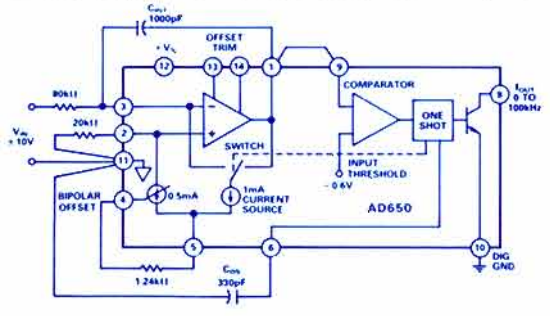


Figure 4. Connections for ±10-V input range (100kHz span).

When the AD650 is used for 1-MHz full-scale output and 0 to 10-volt input, R is equal to 16.9 kΩ* and C_{os} is 51 pF (typically mica or low-drift ceramic). The wiring must include the bypass

*Standard 1% value.

capacitors (including perhaps a 10μF instead of the 1μF shown in Figure 3) and the 510-ohm output-collector load. In general, proper R-F techniques must be observed when operating the circuit at 1 MHz. Lead lengths must be kept as short as possible—especially on the one-shot and integration capacitors, and at the integrator's summing junction.

A 3.6 kΩ pulldown resistor from the output of the integrating amplifier to $-V_s$ is used to draw extra current to reduce the op amp's output impedance and improve its transient response. An offset-trim circuit might be helpful; it consists of a 20-kΩ trim potentiometer connected between the two trim terminals, with the wiper connected to +15 volts via a 200 kΩ series resistance. Although the device is operating at its rated performance limit, nonlinearity is guaranteed less than 0.1% and gain-temperature coefficient ranges from −0.04%/°C at temperatures less than 0°C to +0.01%/°C in the vicinity of +100°C. Gain tempco is considerably lower for less-demanding output ranges, e.g., just a few ppm/°C for 10kHz full scale.

Component Selection. The two parameters available to the user to control full-scale frequency are R and C_{os}. The "swing" variable that is also affected by the choice of R and C_{os} is nonlinearity. The selection guide of Figure 5 shows this quite graphically. In general, larger values of C_{os} and lower full-scale input currents (higher values of R), provide better linearity. In Figure 5, the implications of the four different choices of R are shown. For a full-scale output of 100 kHz, you can see that, among the available choices, R = 20 kΩ and C = 620 pF gives the lowest nonlinearity, 38 ppm. Also, if you wish to use the highest frequency that will give the 20 ppm minimum nonlinearity (for dynamic range and speed of response), it is about 33 kHz (40.2 kΩ and 1000 pF).

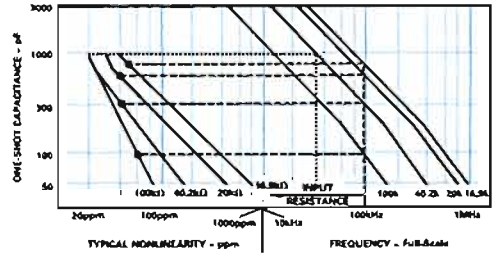


Figure 5. Design considerations for R and C_{os}.

The AD650 can also be used as a frequency-to-voltage converter, e.g., in building a tachometer. Figure 6 is a functional diagram of the basic connections. Each input pulse causes the comparator to trigger the one-shot, which produces a 1 mA × T_{os} increment of charge, which is averaged by the R-C_1 lag circuit. The averaged output of the op amp is proportional to the duty cycle, T_{os}/T, and, since T_{os} is constant and T = 1/f, the output is thus proportional to f.

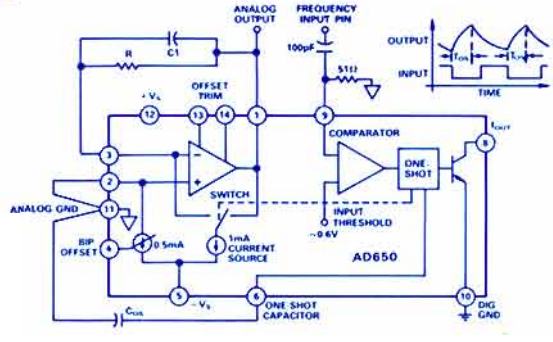


Figure 6. F/V conversion — basic connections.

FAST ADC & DAC FOR TELECOMMUNICATIONS

14-Bit ADC Has T/H, Runs at Word Rates from DC to 125 kHz
14-Bit DAC Has Gated RZ Output, Word Rates up to 200 kHz

The HAS-1409KM and HAS1409AKM* 14-bit hybrid a/d converters—an industry first— are capable of word rates up to 125 kHz. Complete with track-and-hold, each is housed in a single 40-pin DIP package, dissipating only 2 W. The KM has an internal clock, for local adjustment of the word rate, while the AKM employs the system clock to establish its word rate.

The HAS-1409 has been characterized with its companion DAC, the HDD-1409,* for assurance of the ac performance needed for use in frequency-division multiplex/time-division multiplex (FDM/TDM) transmultiplexer systems. Although specifically designed for those kinds of applications, its high speed and low distortion are of value for other forms of signal processing, such as computerized-axial-tomography (CAT) and nuclear-magnetic-resonance (NMR) scanners and pulse-code modulation.

The HDD-1409KM, in a 32-pin DIP, is a voltage-output DAC capable of accepting data at update rates from dc through 200 kHz. Complete with input registers, current-output DAC, switching circuits, and output amplifier, its output range is ±5 V, with 600-ohm output impedance; the deglitched return-to-zero (RZ) mode allows the optimum duty cycle to be selected for FDM/TDM and PCM applications.

This new family offers system designers high speed and 14-bit resolution, plus savings of space, power, and system cost, without sacrificing performance or reliability. Prices for HAS-1409KM/AKM are $380/$365 (1-24), and for HDD-1409KM, $135.

16-BIT ADC

High-Performance ADC1143 Is Fast, Compact, Low-Power

The ADC1143* is a complete 16-bit successive-approximation a/d converter in a compact 2" × 2" × 0.4" module.

Its low power consumption, 175 mW at $V_s = \pm 15V$ and $V_l = +5V$, and its ability to operate with V_s as low as ±11.4 V (dissipating only 150 mW) are well-suited to portable data-acquisition systems, where remote collection of low-level, wide-dynamic-range signals is required. Examples include seismic data acquisition and the design of scientific instruments for field applications.

Data is available in both serial and parallel form; and there are five selectable input-voltage ranges (+5 V, +10 V, +20 V, ±5 V and ±10V), providing output data in binary, offset binary, and 2's complement coding.

The ADC1143 is available in two selection grades: the K provides the highest accuracy (±0.003% FSR) with 100µs conversion time; the J provides faster conversion (70 µs) at ±0.006% FSR.

Brief Specifications	ADC1143J	ADC1143K
Integral Nonlinearity (%FSR, max)	±0.006	±0.003
Diff. Nonlinearity (%FSR, max)	±0.006	±0.003
Diff. Nonlinearity Tempco (ppm max)	±2	±1
Conversion Time (µs max)	70	100
Offset Tempco (µV/°C max)	±40	±40
Bipolar Offset Tempco (ppm/°C max)	±9	±9
Gain Tempco (ppm/°C max)	±12	±12
Price (100s)	$149	$172

Typical applications include seismic data acquisition, oil-well instrumentation, portable industrial scales, portable test equipment, and robotics.

10-BIT-PLUS-SIGN ADC CONVERTS IN 80µs

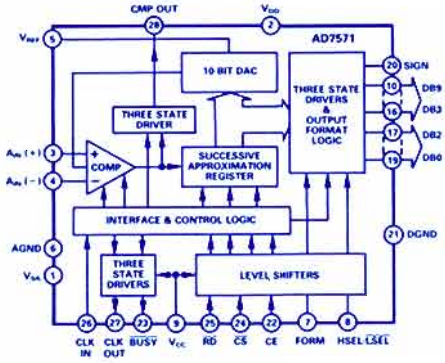
Monolithic CMOS AD7571 Has Differential Inputs
Plus Versatile µP Interface, Parallel and Serial Outputs

The AD7571* 10-bit-plus-sign CMOS a/d converter can convert in 80µs (max), nearly 2 ½ times faster than currently known competing ADCs. Differential inputs provide it with full ±10-volt bipolar input signal range, and its output is available either in parallel—as one or two bytes for 16- or 8-bit µPs, or serially, via 3-state buffers.

Its low-power CMOS construction and fast conversion time are well-suited for battery-powered applications; and a serial data stream is available, synchronizable to the internal clock, for remote applications calling for opto-isolated transmission.

Key performance specs include ±½-LSB maximum relative-accuracy error (K, B, T), and no-missing-codes over temperature. Common-mode error is specified at ±0.1 LSB/V—i.e., 1 LSB, or −60 dB, at full scale.

The AD7571 requires only a single-polarity reference to accept bipolar inputs; and it can operate from a single positive power supply for positive input signals. For bipolar operation, ±15V and +5V are required. It will operate with its on-chip clock, or—if desired—with an external clock; and it is TTL- and CMOS-compatible.



Relative accuracy error over temperature is guaranteed at ±1 LSB max for J, A, and S grades, and at ±½LSB max for K, B, and T (packaged in plastic, cerdip, and side-brazed ceramic). Prices (100s) start at $19.50.

*Use the reply card for technical data.

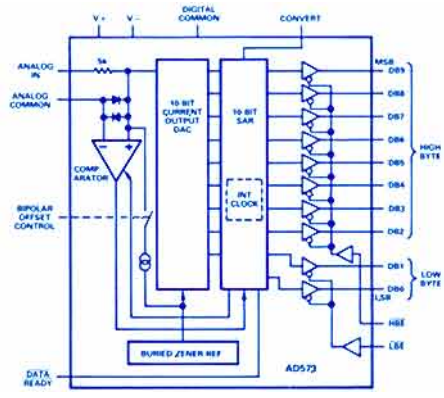
Low-Cost µP-COMPATIBLE IC 10-BIT A/D CONVERTER

AD573 Includes Reference, Clock, Comparator, Buffer
Converts in 15 µs, Has No Missing Codes Over Temperature

The AD573* complete monolithic 10-bit ADC, consists of a DAC, voltage reference, clock, comparator, successive-approximation register (SAR), and 3-state buffers. No external components are needed for a full-accuracy 10-bit conversion in 15 µs (30 max).

The AD573 interfaces to many popular microprocessors without external buffers or peripheral interface adapters. The 10 bits of output data can be read in one or two bytes.

Operating on supplies of +5 V and −12 V to −15 V, the AD573 will accept analog inputs of 0 to +10V (unipolar) or −5 V to +5 V (bipolar), as determined by hard-wiring the state of a single logic pin. A positive pulse on the CONVERT line initiates the 15 µs conversion cycle. $\overline{\text{DATA READY}}$ indicates completion of the conversion. HIGH-BYTE ENABLE ($\overline{\text{HBE}}$) and LOW-BYTE ENABLE ($\overline{\text{LBE}}$) control the upper 8-bit and lower 2-bit 3-state output buffers.



Two versions (AD53J/K) are offered for the 0°C to +70°C temperature range. The AD573S guarantees 10-bit accuracy and no missing codes from −55°C to +125°C and is also available in a MIL-STD 883 version.

The AD573S is furnished in a 20-pin hermetically sealed ceramic DIP. The AD573J and AD573K are available in a choice of plastic or ceramic packaging. Prices start at $15.90 (100s, AD573JN—plastic).

MONOLITHIC VOLTAGE-OUTPUT AD DAC80

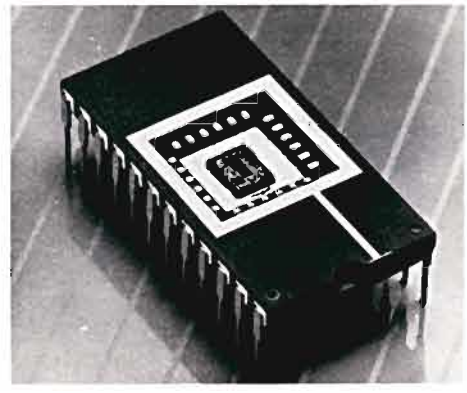
Industry's First DAC80 in a Plastic Package
Lowest Power Dissipation (450 mW max)

The AD DAC80* is a new monolithic 12-bit voltage-output d/a converter for which second sources already exist in hybrid form. It is distinguished among them by its 35% lower power dissipation than the closest competitor (450 mW maximum) and its availability in a low-cost plastic package, priced from $16.95 in 100s.

Operating supply voltages include both ±12 V and ±15 V; thus, AD DAC80N can replace either standard or "Z" versions directly. Its internal buried-Zener reference makes available 2.5 mA for use elsewhere.

In fast applications, the AD DAC80's guaranteed maximum settling time is 3 µs to ±0.01%, for a 10-V full-scale output step, the fastest for any DAC80 or equivalent.

The AD DAC80 meets or exceeds the specs of its namesakes; for example, it guarantees: monotonicity from 0°C to +70°C; maximum linearity error at ± 1/2 LSB over



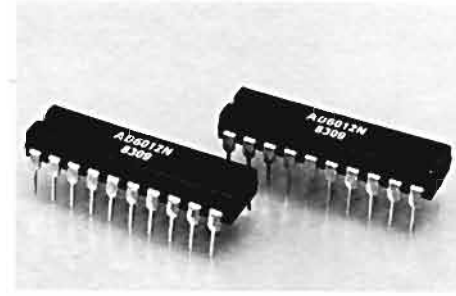
temperature; maximum unipolar and bipolar offset drifts at ±3 and ±10ppm of full-scale reading per °C; and maximum gain drift at ±30ppm/°C. The device will operate over the −25°C to +85°C range with only slightly degraded specifications.

A choice of jumper-programmable full-scale output ranges is available: 0 to +5 V, 0 to +10 V, ±2.5 V, ±5 V, and ±10V. It is housed in a choice of plastic or hermetically sealed ceramic 24-pin DIPs.

*Use the reply card for technical data.

AD6012 DAC

12-Bit Second Source
500-ns Settling Guaranteed



The AD6012*, a 12-bit monolithic current-output d/a converter, has a guaranteed maximum settling time of 500 ns and monotonic performance over the temperature range. Housed in a low-cost 20-pin plastic DIP, it is a direct replacement for 6012-type converters from other manufacturers.

Its combination of high output compliance voltage (−5 to +10 V) and high output impedance (typically greater than 10 MΩ) allow the DAC's 4-mA output to drive resistive loads directly without degrading the accuracy of the converter.

Other features of the DAC include a fast-slewing 8-mA/µs reference circuit for high-speed two-quadrant multiplication, complementary current outputs, and a low gain-drift of 10 ppm/°C typical. The AD6012 is compatible with TTL, CMOS, ECL, and HTL logic inputs. The specified temperature range with ±15-V supplies is 0°C to +70°C. The device will operate from −25°C to +85°C, and with supplies from +4.5V/−10.8 V to ±18 V. Available from stock, it is priced at $9.30 in 100s.

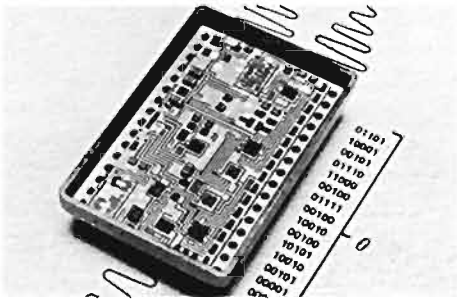
Applications for the AD6012 include vector-scan video displays, process control, and fast a/d converters.

Although 12-bit resolution and monotonicity are essential for a 12-bit DAC, many applications tolerate deviations of a few bits from an ideal straight line. The segmented architecture typical of 6012's allows them to use all-diffused resistors instead of a laser-trimmed thin-film R-2R ladder network. While the result is a maximum relative accuracy error of ±0.05% of full scale, the AD6012 achieves a fully monotonic maximum differential linearity of ±1 LSB over temperature at low cost.

New Product Briefs

HYBRID DIGITAL/RESOLVER CONVERTERS

14- & 16-Bits, With Latched Input Registers
Low-Dissipation Units Operate at Frequencies to 2.6 kHz



Models DRC1765 and DRC1766* are 14- and 16-Bit hybrid Digital-to-Resolver Converters, with latched inputs, housed in a 32-pin package. They modulate an input reference signal to provide outputs proportional to the sine and cosine of a binary digital input word representing angle, for driving radar displays and plotters, and for use in A.T.E. The reference input voltage can be either dc or ac, with sine waves of up to 2.6 kHz.

The upper and lower 8-bit bytes of the 16-bit-wide digital input to the converter can be latched separately, using transparent single-rank TTL-compatible latches, making possible operation with 8- or 16-bit microcomputer buses without extra digital hardware. The devices are available for interfacing optionally with either CMOS or low-power Schottky logic.

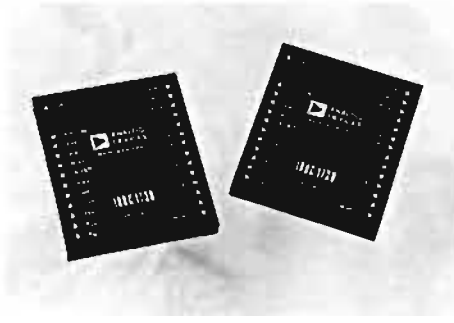
Recommended analog input range is 3.4 V rms; with its inherent scale factor of 2, the analog output is then 6.8 V rms, providing up to 4.3 mA of peak output current at ±10 V.

Typical DC offset is a low ±12 mV max. Settling time to within the accuracy of the converter is 20μs max. The converters can drive resistive, inductive, and capacitive loads (of up to 0.015 μF). The DRC1765 and DRC1766 are available with a choice of accuracy grade: ±2/±4 arc-minute error. Prices (1-9, −55°C to +125°C operation) are $513/$404 (DRC1765) and $603/$513 (DRC1766).

INDUCTOSYN-RESOLVER/DIGITAL CONVERTER

For 12-Bit Linear or Angular Position Measurements
High Performance at Low Cost with Model IRDC1733

The IRDC1733* converts resolver-format (sine and cosine) signals into a 12-bit parallel word. If the inputs come from a resolver, the output represents the angle of a resolver shaft; if the inputs are from an Inductosyn† slider (via external preamplifiers), the output word represents the fractional position of the slider within an Inductosyn pitch (to the nearest 1/4096th, for 12-bit resolution).



A typical application of the IRDC1733 is to furnish position information, in digital form, to a processor in numerically controlled machine tools and robots.

Like the IRDC1730,* introduced here in *Analog Dialogue* 16-1 (1982), the IRDC1733 is a high-speed 12-bit tracking-type converter with transformer-isolated inputs, ripple carry for keeping track of number of pitches or revolutions, 12-bit parallel output, direction output, and a full range of frequency options, from 400 Hz to 10 kHz.

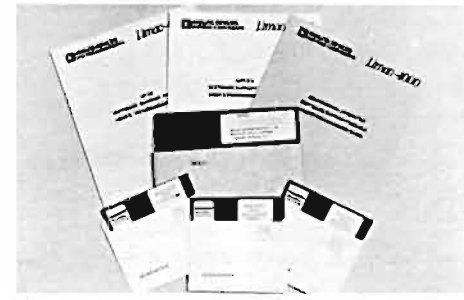
Its accuracy is the same, ±8 arc-minutes, and its tracking rate—depending on the frequency option—is from 60 to 170 rps. It differs only in not having a velocity output. Where this feature is not needed, or can be simulated digitally, the IRDC1733 typically provides a cost saving, compared to the IRDC1730, of 18%. Prices (1-9) for the IRDC1733 start at $273.

*Use the reply card for technical data.

†Inductosyn is a registered trade mark of Farrand Industries, Inc.

μMAC SOFTWARE

Speeds Data Acquisition for DEC, HP, Apple, & IBM PCs



The μMAC-4000*, introduced in these pages in 1981 (Vol. 15, No. 1), is a low-cost, intelligent, expandable, modular measurement-and-control system on a single board. It provides isolation, preamplification, and conversion, as well as both digital and analog signal-conditioning for field-wired signals from sensors. Among its many other functions, it accepts digital inputs and provides a set of digital control outputs.

μMAC-4000 systems employ a powerful command set to communicate with a host computer's 20-mA or RS-232C serial port. As a convenience to users, to make the command set transparent to the programmer, we provide software drivers for many popular computers which might be employed as hosts. For example, AC1820* support packages are for Apple II and Apple IIe computers (DOS 3.3, Applesoft BASIC), AC1818s* are for HP-85/86/87/9915 computers (BASIC), the AC1822* is for IBM Personal Computers (MS-DOS, BASIC), and AC1815s* are for DEC computers—employing RSX-11, RSX-11S, and RT-11 operating systems and BASIC, FORTRAN, or MACRO-11 languages.

Recent improvements and enhancements to μMAC software include:

- Adding a version of the AC1815 to use the DEC RT-11 operating system, handling formatting of the command strings, checksum generation and checking, unpacking the μMAC reply string, status checking, and error handling.
- Improving the AC1820's programs to reduce communication and scan time by factors of at least 3. For example, a 48-channel scan can now be performed in 7.7 seconds, a 12× speedup.
- Adding a version of the AC1818 to handle HP-86 and HP-87 computers.

BROADEST-CAPABILITY BENCHTOP TESTER

LTS-2000 Series Systems Now Test Transistors and Diodes As Well as Linear, Digital, and Data-Conversion ICs

The LTS-2000 Series* of Component Test Systems (including the LTS-2000, LTS-2010, LTS-2012, and LTS-2015), when used with the LTS-2600* Transistor Family Board, can now test a wide variety of transistors—bipolar, MOSFET, and JFET—plus constant-current and Zener diodes and optocouplers in semiconductor manufacture, incoming inspection, and component-evaluation applications.

Covering a wide dynamic range, the test system can force or measure voltages from 10 mV to 600 V, and currents from 100 pA to 20 A. Test accuracy is to within ±0.25% to ±2%, depending on device type and measurement range. The LTS-2600's on-board μP handles pulse generation and timing; it also coordinates housekeeping and safety functions during testing. Compatible with automatic component handlers and wafer probers, the LTS-2600 brings guarded Kelvin test capability right to the contactor or probe.

Test programs may be created with ADI's fill-in-the-blanks CREATE technique, using standard parameters, or in BASIC.

With the introduction of the LTS-2600, and the availablity of six other family boards, these systems offer a very low cost-to-test ratio over the full range of semiconductor components. Electronic equipment manufacturers can now utilize one system for the majority of their component inspection needs. In addition to precision testing, it makes available automatic data reduction and statistical analysis, permitting component test reports to be generated easily with clarity. ▶

BENCHTOP TESTER

Flexible and Low-Cost Tests ICs and Discretes

The LTS-2012* Component Test System, with 16-bit overall system measurement accuracy and compatible with all LTS family-test boards, offers dual floppy disk drives, integral alphanumeric keyboard and display, and both BASIC and menu-style programming.

It provides test and measurement capability for linear, data-conversion, and digital integrated circuits, plus transistors, diodes—and other active and passive components—at low cost. Fully compatible with automatic handlers and probers, and capable of testing at speeds comparable to those of mainframe testers, the LTS-2012 is well-suited for incoming inspection and semiconductor production testing.

In addition, its dual disk drives, with 368 kilobytes of storage, and its standard software for lot yield analysis, lot parametric distribution, and data-logging combine to make it a powerful evaluation system. A large library of turnkey test programs, written to manufacturers' specifications, is available for many different device families. It can verify its own internal accuracy using a unique calibration board with an NBS-traceable HP 3455A or 3456A DVM.

The LTS-2012's architecture, like that of general-purpose mainframe testers, has source and measurement capabilities optimized for particular families of devices through the use of dedicated family boards and socket assemblies; thus, the LTS-2012 can be expanded to test a growing number of device types and adapted for custom device testing at the user's option.

The system's base price, without specific family board and socket-assembly hardware, is $31,500. The cost of individual family test capabilities ranges from $500 to $6000. ▶

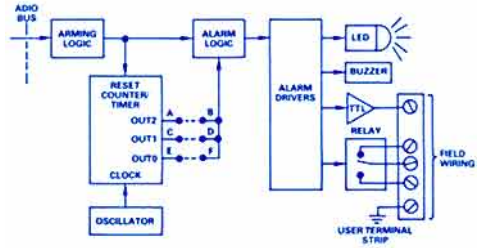
AUTOMATIC SYSTEM-MALFUNCTION DETECTION

MACSYM's WDT01 Watchdog Timer Provides Alarm and Switching Monitors Critical Control Loops; Switches to Backup Mode

The WDT01* Watchdog Timer card for MACSYM systems is a hardware-programmable interval timer that requires periodic resetting by the user's software within its programmed time-out period. If the software should fail to reset the WDT01 in time (due to a hardware malfunction or system software fault), the WDT01 will independently generate an alarm signal. Cycle times are strap-selectable for intervals of 0.5, 8.0, and 64 seconds, for order-of-magnitude matching to system speed.

For example, a task (taking advantage of MACSYM's multitasking feature) may be set up to periodically monitor a number of system variables and their trends and reset the timer if they are all within preset limits. Otherwise, the alarm will go off at the next timing event.

Audio and visual alarm are inherently available, in the form of a board-mounted hardware-enabled buzzer and a card-edge mounted LED. In addition, both a TTL signal and a Form C (SPDT) reed-relay contact are available to produce specific system responses to the alarm. A set of board-mounted screw terminations are provided for direct interface to high-power mechanical and solid-state relays.



Besides automatic detection and alarming of system failures, typical applications include automatic switchover to manual backup equipment and independent monitoring of critical control loops. ▶

*Use the reply card for technical data.

WORTH READING

Some Technical Books ADI Engineers are currently reading*

Solid-State Radio Engineering, by Herbert L. Krauss, Charles W. Bostian, and Frederick H. Raab. John Wiley & Sons, Inc. (New York), 1980. "A Fundamental treatise on radio-frequency circuit design. Wide-ranging tutorial approach. A good way for the practicing engineer in other specialties to branch out into r-f circuits."

The 8085 Microprocessor – Fundamentals and Applications (Hands-On), by Dr. Howard Boyer. Two volumes, paperback. Microprocessor Training, Inc. (New York), 1980. "Useful for learning about how to interface real-world types of devices to a microprocessor to make it useful as a controller, etc. Good tutorial."

STD Bus Interfacing, by Christopher A. Titus, Jonathan A. Titus, and David G. Larsen. Howard W. Sams & Co., Inc. (Indianapolis), 1982. "A practically oriented description of the STD bus and how to use it, with many examples of both hardware and software."

Technical Articles by ADI People

Not available as reprints unless preceded by an asterisk (*).

"Understanding Noise," by Alan Rich, *Electronics Test*, May, 1983.

"RMS Audio AGC Amplifier," by Charles Kitchin, *Electronic Design*, April 28, 1983.

"Multistage Error-Correcting ADCs," by Sid Kauffman, *Electronic Products*, April 18, 1983.

"Control Software for Factory Automation," by John Sylvan, *Computer Design*, April 21, 1983.

*"Four DACs on a Chip Ease Multiconverter System Design," by Paschal Minogue, Mike Byrne, and John Jennings, *Electronic Design*, June 9, 1983.

"Resolvers and Synchros for Microcomputers," by Ed Friedman, *Machine Design*, January 6, 1983.

"Building a Data Acquisition System from Board Level," by John Sylvan, *Digital Design*, April, 1983.

NEW PUBLICATIONS FROM ANALOG DEVICES

Available upon Request

Periodical: *The Measurement and Control Digest: Applications/User Feedback/Information*, published by the Measurement and Control Division of Analog Devices. The most-recent issue (Volume 3, Number 2, July, 1983), with 20 pages, features industrially hardened signal conditioning (the 3B Series) and includes application articles on common-mode rejection, new features of and enhancements to the MACBASIC 3 language, creating SDF-compatible files, VARILOG – a semilog graphics plot, OKIDATA block graphics, and other topics. Other departments include new-product information, customer-service notes, and classified ads.

*We'd like to hear about recent technical books that *Analog Dialogue* readers have found interesting and helpful. Drop us a note with title, author, publisher, and copyright date, plus a one- or two-sentence comment on what it's about and why it's useful. These books are not available from ADI.

"A Cookbook to Digital Filtering and Other DSP Applications," a collection of reprints of papers that originally appeared in EDN magazine during 1983. Topics include FIR filtering, temporal averaging, multiband filters, IIR filtering, and implementing modern control theory with DSP.

Brochure: *MACSYM 16-Bit Measurement-and-Control Systems – Powerful enough for 700 I/O points, yet cost-effective for 7*, describing the MACSYM 150/350 measurement-and-control computer system.

MORE AUTHORS

(Continued from page 2)

Scott Wurcer (page 6) is a Design Engineer at Analog Devices Semiconductor. A native of Milwaukee, Wisconsin, he graduated from M.I.T. with a BSEE in June, 1973. While at M.I.T., he worked in the X-Ray Astronomy Group at the Center for Space Research. He has been employed at ADS since 1974, in various engineering positions. He is a member of IEEE.

Bill Windsor (page 12) is a Marketing Specialist at Analog Devices' Digital Signal Processing Division. Before joining ADI, he worked at Honeywell's Small Systems and Terminals Division, designing custom minicomputer hardware. Bill holds a BSEE degree from M.I.T. and an MBA from the Harvard Business School. His spare-time activities include running, backpacking, and squash.

Paul Toldalagi (page 12), a Senior Staff Engineer at Analog Devices, is a project manager in the DSP division. Previously, he was with Scientific Systems, Inc. Paul earned MS and PhD degrees in electrical engineering at M.I.T. and an MS in physics at Université Paris XI France. He is a member of IEEE, the American Meteorology Society, and Sigma Xi, and his hobbies include classical music, meteorology, and finance.

Larry DeVito (page 20) is a Design Engineer at ADS. An M.I.T. graduate, he obtained the SB in 1975, and both the SM and EE in 1977. At M.I.T., he worked in the Crystal Physics Laboratory at the Center for Materials Science and Engineering, developing sputtered X-Ray phosphors. After working for several years with the Sprague Electric Company as an IC design engineer, he joined ADS in 1980. His hobbies include reading, gardening, and amateur radio.

Potpourri

An Eclectic Collection of Miscellaneous Items of Timely and Topical Interest. Further Information on Products Mentioned Here May Be Obtained Via the Reply Card.

IN THE LAST ISSUE . . . (Volume 17, Number 1, 1983 -- 28 pages):

Low-Power Digital Signal-Processing ICs (8- and 16-bit Multipliers & Multiplier-Accumulators)
Shielding and Guarding (How to exclude interference-type noise)
Fast, Flexible Switched Dual-Input IC Op Amp and Comparator for Modulation, Demodulation, Synchronous Detection, etc. (AD630)
Level-Independent Automatic Gain Control with IC LOGDAC™
12-Bit, 10-MHz Analog-to-Digital Converter (CAV-1210)
Alarm Limit Subsystem is Modular and Rugged (4B Series)
Test MOS and Bipolar SSI & MSI Digital ICs with LTS-2000 Test Systems (LTS-2500 Digital Device Family Board)
Understanding the MACSYM 150/350 Software
New-Product Briefs:
- Ultrafast 8-Bit Monolithic DAC Settles in 5 ns (AD9768SD)
- High-Speed Single and Dual IC Sampling Comparators (AD9685,AD9687)
- Video-Speed 100-mA Op Amp Settles to 0.1% in 80 ns (HOS-060)
- MULTIBUS-Compatible 12-Bit Analog I/O Boards (RTI-11, -724 & -732)
- 16-Bit Synchro/Resolver-Digital Converters (SDC1721, RDC1721)
- 18-Bit DAC Has Low Cost, Linearity to 0.00076% (DAC1146)

Editor's Notes, Authors, New Literature, Potpourri, Advertisement.

Errata: Page 3, "In This Issue," year is 1983 . . . Page 3, middle of line 4: Delete "and". . . Page 7, Figure 9: $Y_{256} - Y_{255}$ instead of dash (This lets you interpolate the last 255 points from FF01 to FFFF. Y_{256} is the extrapolated value Y would have if X_{256} existed) . . . Page 15, Figure 3: Input waveforms are interchanged; square wave is lower signal.

DATA-SHEET UPDATE . . . 12-page Data Sheet Describes MACSYM 150 Series 100 I/O Cards. Includes AIM100 Analog Input, TIC100 Thermocouple Input, DIO100 Digital Input/Output, DSI100 Serial Interface, ACP100 IEEE-488 Interface, and BNK101 Blank Card . . . 1982 DATABOOK, Volume 2, page 5-22, Figure 24, and page 5-30, Figures 12 and 13, pins 4 and 5 of Model 281 are interchanged (pin 4 is SYNC IN and pin 5 is SYNC OUT) . . . In recent printings, salient errors were made in the AD7520/AD7521 Data Sheet ("Bug" on inner margin of last page is C218c-5-2/83) and AD7530/AD7531 Data Sheet (C335d-5-1/83). They will be replaced; please dispose of them and request new ones . . . AD579 Data Sheet: If "bug" on inner margin of page 6 is prefixed "C667", request the latest data sheet, with prefix "C667a". Changes are: (1) Figure 4, Bipolar Input Connections, tie trim resistor (pin 26) to REF OUT (pin 24), not ground; (2) Pages 2 and 6, delete AD579BD and AD579ZBD for new designs; (3) Page 2, Power Supply Requirements, change +5V current to 100 mA typ, 150 mA max; (4) Page 2, Temperature Coefficients, all grades have the same tempco specs - new specs are: Gain, 40 ppm/°C max, Unipolar Offset, 15 ppm/°C max, Bipolar Offset, 20 ppm/°C max . . . AD2700: Don't double-count the error at 25°C; the ±5.5 mV T_{min} to T_{max} box-limit drift spec includes the maximum +25°C error.

PRODUCT NOTES . . . AD594 calibration specs have been modified for a more precise gain and offset match to Type J thermocouple characteristics, 0°C to +50°C. New closed-loop gain is 193.4 V/V (vs. 192.3) and input offset voltage is (Temperature x 51.7 uV/°C), instead of (Temperature x 52 uV/°C). The AD594's output voltage becomes: 193.4 x (Type J voltage + 16 uV) . . . AD522BD spec changes: Input Bias Current, initial (max @ + 25°C), 25 nA (was 15 nA); vs. temperature (typical), 100 pA/°C (was 50 pA/°C). Input Offset Current, initial (max @ 25°C), 20 nA (was 10 nA); vs. temperature (typical), 100 pA/°C (was 50 pA/°C) . . . One-watt dc-to-dc converters, types 959 through 964, are available in two new no-cost optional forms: (1) With "P" suffix, a balance pin is provided for external adjustment of the balance between the dual outputs, typically ±1%; (2) with "R" suffix, an alternative pin configuration is provided for compatibility with V-PAC™ regulated dc/dc converters (pinout "B") from Reliability, Inc.

PATENT . . . U. S. Patent 4,383,222, to William H. Morong, III, for "Half-Wave Signal Isolator with Compensator Means to Reduce Temperature-Dependent Effects."

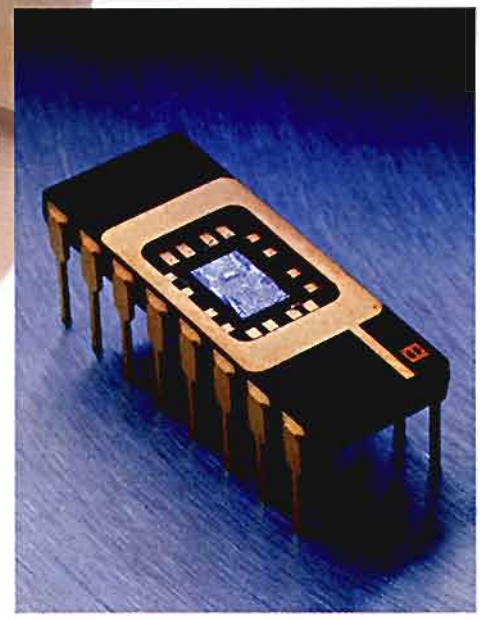
The AD524. You can't build or buy a better I/A. And you won't believe the price—under $10!

The struggle to come up with the right I/A for your application is over. Never again will you have to design around two or three op amps and a handful of resistors, or pay the high price of a hybrid, or settle for a monolithic IC with less-than-satisfactory specs. Our new monolithic AD524 gives you all the performance and functionality you'll ever need in an I/A. And you can get it all at a price that's designed to make you forget the past.

The AD524 has the best specs attainable in an I/A, whether you're talking monolithic, hybrid, or discrete. Nonlinearity to ±0.003%. Input offset voltage drift of ±0.5 μV/°C. Gain error of ±0.02%. Common mode rejection of 130 dB. 0.3μV peak-to-peak low frequency noise. Your dream specs are now a reality!

And the AD524 couldn't be easier to use. Pre-trimmed on-chip gain resistors give you pin-strappable gains of 1, 10, 100, or 1000. The AD524's inputs are internally protected against overvoltage (power on or off), eliminating the need for external diode clamps. And sense and reference inputs let you make sure that the output is accurately presented to the load.

So if you're still rolling your own, or considering the National LM363 or the Burr-Brown INA101, find out just how good an instrumentation amp can be. Call Don Travers or Doug Grant today at 617-935-5565, or write Analog Devices, Inc., P.O. Box 280, Norwood, MA 02062.



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